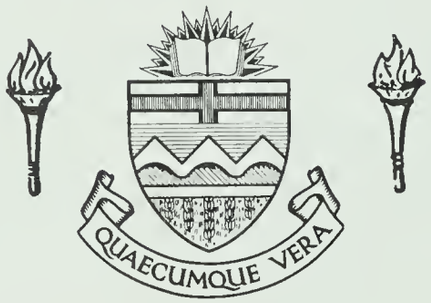

University of Alberta
Printing Department

A FLUIDIC INTEGRATOR

THE UNIVERSITY OF ALBERTA

A FLUIDIC INTEGRATOR

by

WILLIAM G. GULLAND

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

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EDMONTON, ALBERTA

JUNE, 1967

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UNIVERSITY OF ALBERTA

FACULTY OF GRADUATE STUDIES

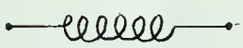
The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled A Fluidic Integrator submitted by William G. Gulland in partial fulfillment of the requirements for the degree of Master of Science.

LIST OF SYMBOLS

Passive Fluidic Devices

Resistor

Capacitor

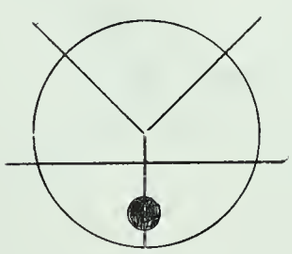


Inductor

Active Fluidic Devices

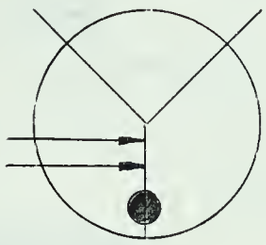
Proportional differential amplifier without "centre-dump"

Proportional differential amplifier with "centre-dump"

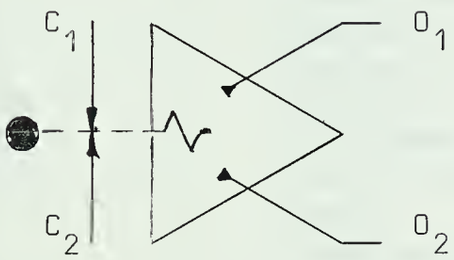


Bistable device. Load insensitive.

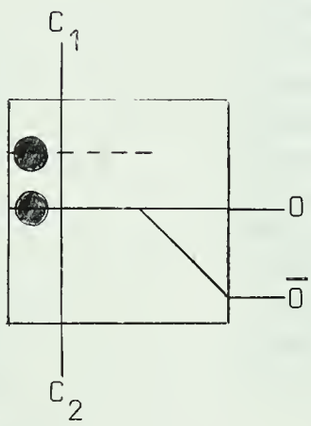
Bistable device. Load sensitive.



OR-NOR logic gate

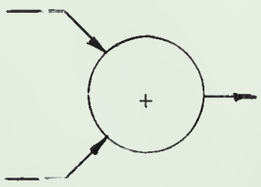


Differential Operational Amplifier.
C_1 high, O_2 high.

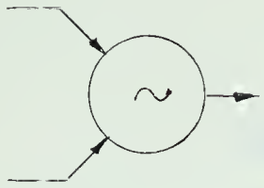


Schmitt Trigger.

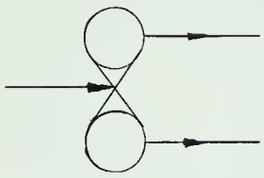
Logic Cates



OR gate



NOR (inversion) gate



Toggle flip-flop

Abbreviations

C	Capacitance
CU	Capacitance Units
dB	Decibels
D to A	Digital to Analogue
G(s)	A Transfer Function
H. F.	High Frequency
Hz	Hertz
IU	Inductance Units
L	Inductance
P	Pressure
psi	Pounds per Square Inch
psig	Pounds per Square Inch Gauge
psid	Pounds per Square Inch Differential
PWM	Pulse Width Modulator
Q	Flow Rate
R	Resistance
RU	Resistance Units
s	Laplace Operator
sci	Standard Cubic Inches
scis	Standard Cubic Inches per Second

Subscripts

c	Control
d	Differential
f	Feedback
i	Input
l	Left
o	Output
p	Positive Feedback
r	Right
s	Supply
t	Load

ERRATA

Page	Line	Remarks
33	18	For "has" read "bias"
43	10	For "alternating" read "attenuating"
48	18	For "length" read "value"
68	13	For "in^5/lb" read "$in^5 sec^2/lb$"
69	Inductance	For "in^5/lb" read "$in^5 sec^2/lb$"

ABSTRACT

This thesis describes a design for a fluidic integrator having infinite hold time for performing analogue computation on pneumatic signals.

Lack of fluidic equivalents for certain electrical circuit elements made it necessary to design a system employing analogue to digital conversion, digital integration and digital to analogue conversion. The circuits to accomplish each of these operations are described.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Fluid Amplifiers

It was late in 1959 that the first announcement was made by the Diamond Ordnance Fuze Laboratories of the development of devices producing amplification of signals transmitted by a fluid medium, without the use of mechanical moving or deformable parts. (Ref. 1) Since that time research and application programmes have been set up by government and private organizations to develop and apply these devices. In the search for units having desired specific characteristics a number of different fluid dynamics phenomena have been exploited. The operating principles of the devices used in the construction of the system described in this thesis are discussed in Appendix A.

A number of different generic adjectives have been proposed for these devices, but none has been given the authority of standardization. The one which has become most popular, largely due to its adoption by "Control Engineering," a technical periodical of wide circulation, and the one which will be used in this thesis is "fluidic." The science (or art!) of their development and application is termed "fluidics."

1.2 The Integrator Problem

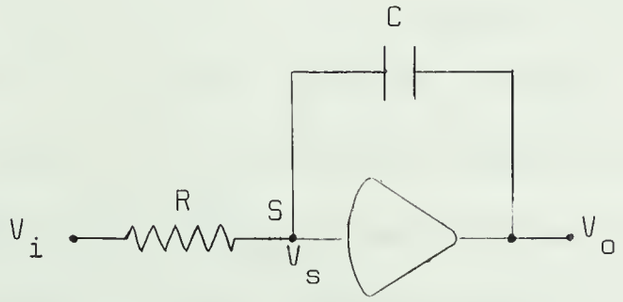
In analogue computation one of the fundamental operations to be performed is that of integration, and if fluidic analogue systems are to be built, it is necessary to have available a satisfactory fluidic integrator. For example, one frequently employed component in control

systems is the Proportional-Integral-Derivative (PID) Controller whose transfer function is of the form:-

$$G(s) = K_p\left[1 + \frac{K_i}{s} + K_D s\right] \qquad (1.1)$$

i.e. its output is the sum of terms proportional to the input, the time integral of the input and the derivative of the input. The input to such a component is normally the error signal of the overall loop. The integral or "reset" term serves the function of zeroing steady state error. Pneumatic controllers with such a transfer function have been available for years, but all those currently available have one common shortcoming; they utilize moving or deformable parts. They are thus subject to wear, which places a limit upon their reliability. Fluidic devices do not have this limitation, and the development of a fluidic integrator is the first step towards the implementation of a more reliable PID pneumatic controller.

It has been stated in the literature that fluidics is capable of performing the same operations as electronics. If this were the case then the construction of a fluidic integrator would be a comparatively simple matter, since the electronic circuit consists of D.C. amplifier of very high gain with the input fed through a large resistor, and the output fed back through a capacitor (Fig. 1.1).



Electronic Integration Circuit Fig. 1.1

Since the input impedance of the amplifier is very high, there is no flow of current into the amplifier input, and the sum of the currents through the input resistor, R, and the feedback capacitor, C, to the node, S, the summing junction, is zero. The very high gain of the amplifier means that $V_s \doteq 0$. The input - output relationship is therefore:-

$$\frac{V_i(s)}{R} + V_o(s)Cs = 0 \qquad (1.2)$$

$$\frac{V_o(s)}{V_i(s)} = G(s) = -\frac{1}{sCR} \qquad (1.3)$$

That is, the output is proportional to the negative of the time integral of the input.

Unfortunately reliable fluidic equivalents do not exist for two of the components of this circuit. As far as the passive components are concerned the resistor presents no problems (Appendix B). However, there is no fluidic equivalent of the electrical point-to-point capacitor; that is, a capacitor of which both sides can have a potential other than ground. A volume forms a fluidic capacitor, but with one side always grounded, fluidic ground being the ambient fluid. Even were such a capacitor available, however, problems would still be encountered with the active element, the operational amplifier. Even the electronic integrator will have a finite, allbeit very long, leakage time constant. It is the combination of high gain and high input impedance which ensures that this time constant is long. A fluidic amplifier with gain and input impedance of the necessary magnitude is not at this time readily available, although one device, the Direct Input Modulator approximates the specifications (Ref. 2).

There does remain one purely analogue approach to the construction of a fluidic integrator. Theoretically, it should be possible to realize the "Bootstrap Integrator", described in Appendix D, with existing types of

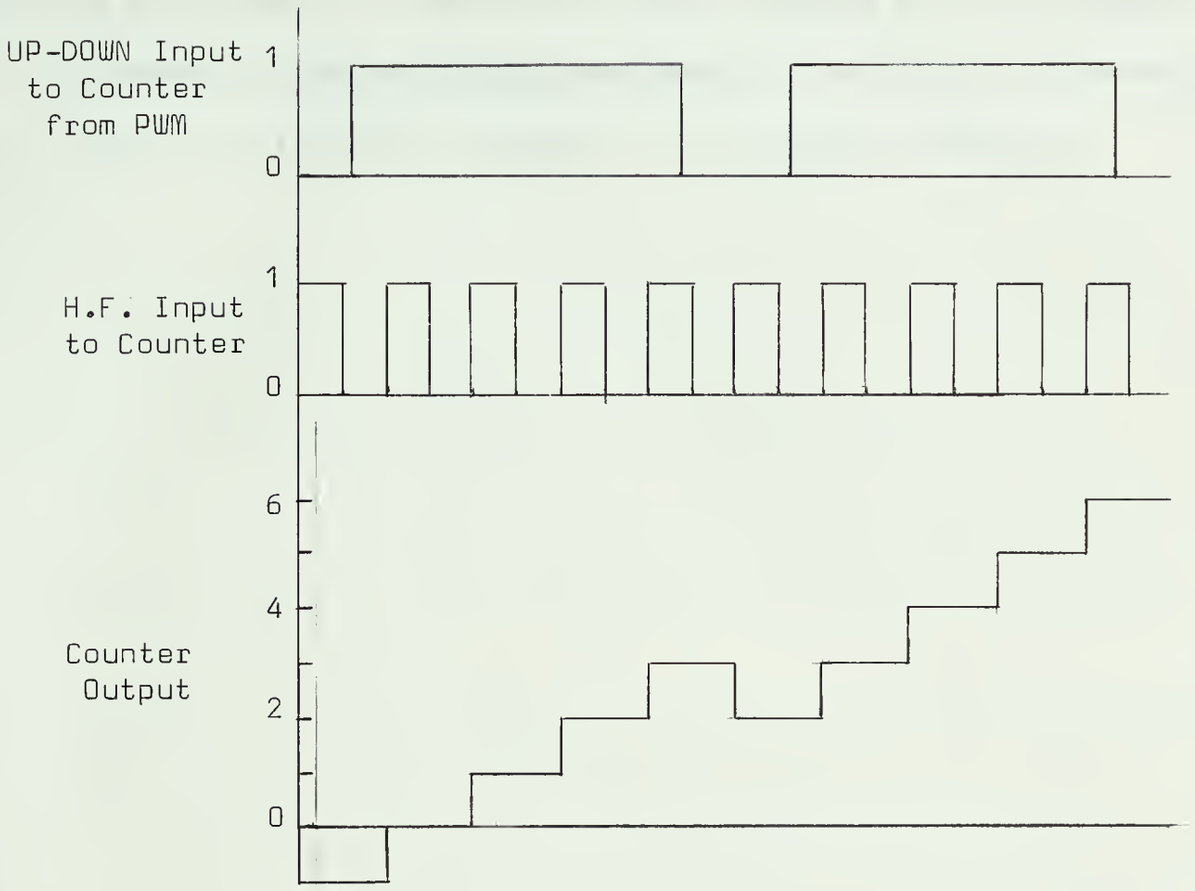
components. However, the practical problems of adjustment of such an integrator were found to be great.

The alternative to a purely analogue system is to perform an analogue to digital conversion and digital integration followed by digital to analogue conversion. In such a system the analogue signal is sampled at intervals, converted to digital form, and successive digital samples are summed to yield the digital integral. Provided that the sampling period is sufficiently short compared with the time constants of the rest of the system (e.g. the plant time constants in the case of the PID controller), such a system need not be at a disadvantage in comparison with a continuously acting system. This was the approach adopted for this project.

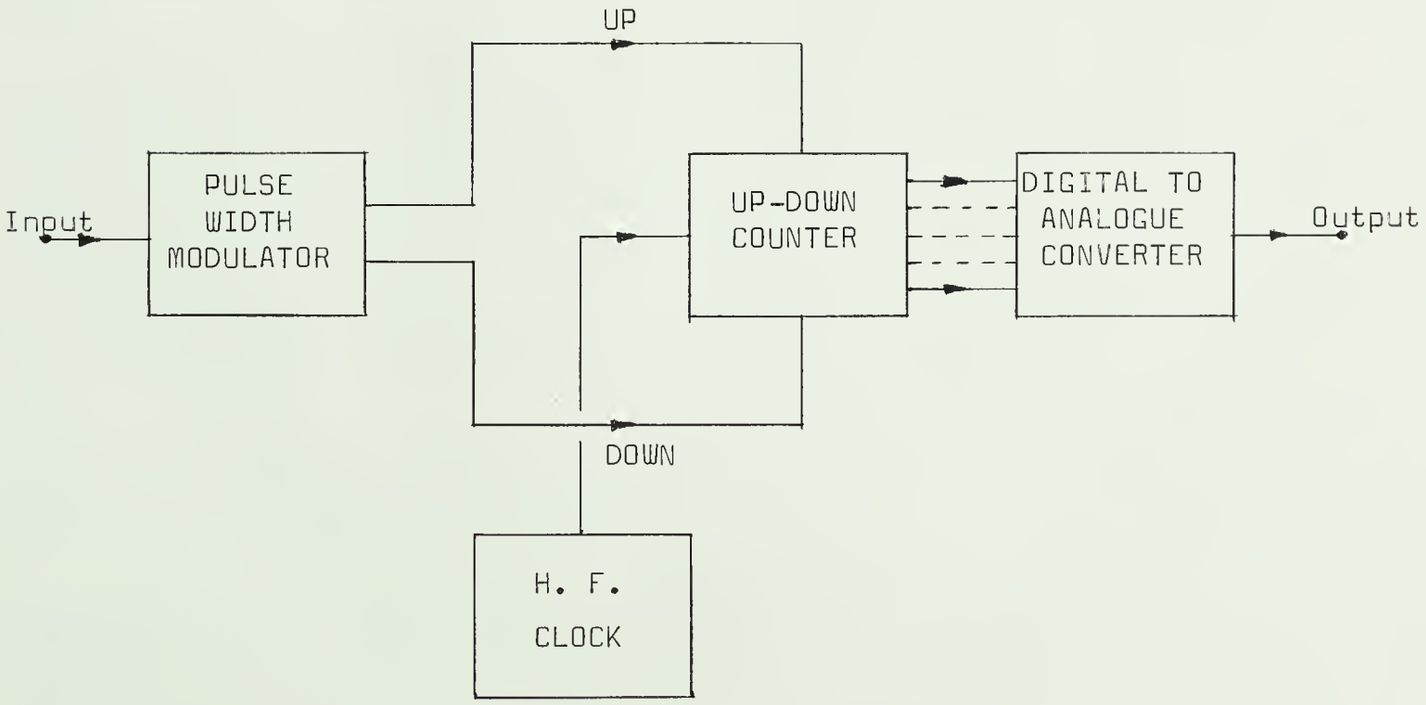
1.3 Outline of System Operation

The sampling technique adopted was pulse width modulation (PWM). In this approach the width of pulses produced by the modulator is made to vary about a mean, being made proportionately longer for positive input and shorter for negative input. The conversion of the information in the PWM signal to digital form and the summation of the samples is then performed simultaneously by using ON and OFF PWM pulses as the direction control of an UP-DOWN counter, into which higher frequency pulses are being fed. During the ON period the counter will count up, during the OFF period the counter will count down. If the ON period is longer than the OFF period the output of the counter will increase during that cycle, and vice versa. Fig. 1.2 illustrates the process.

The counter does not move steadily in one direction, but has a period of counting UP, and one of counting DOWN, during each PWM cycle, producing ripple on its output. This is minimized by making the period of the high frequency pulses only a few times shorter (~10) than the period of the



Digital Integration Process Fig. 1.2



Integrator Circuit Schematic Fig. 1.3

PWM pulses, so that the numbers added to the counter during each ON period and subtracted during each OFF period are small compared with its capacity.

This process is similar to that performed by the Digital Differential Analyzer. Fig. 1.3 is the block diagram of the complete integrator.

CHAPTER 2

CONSTANT FREQUENCY SQUARE WAVE GENERATORS

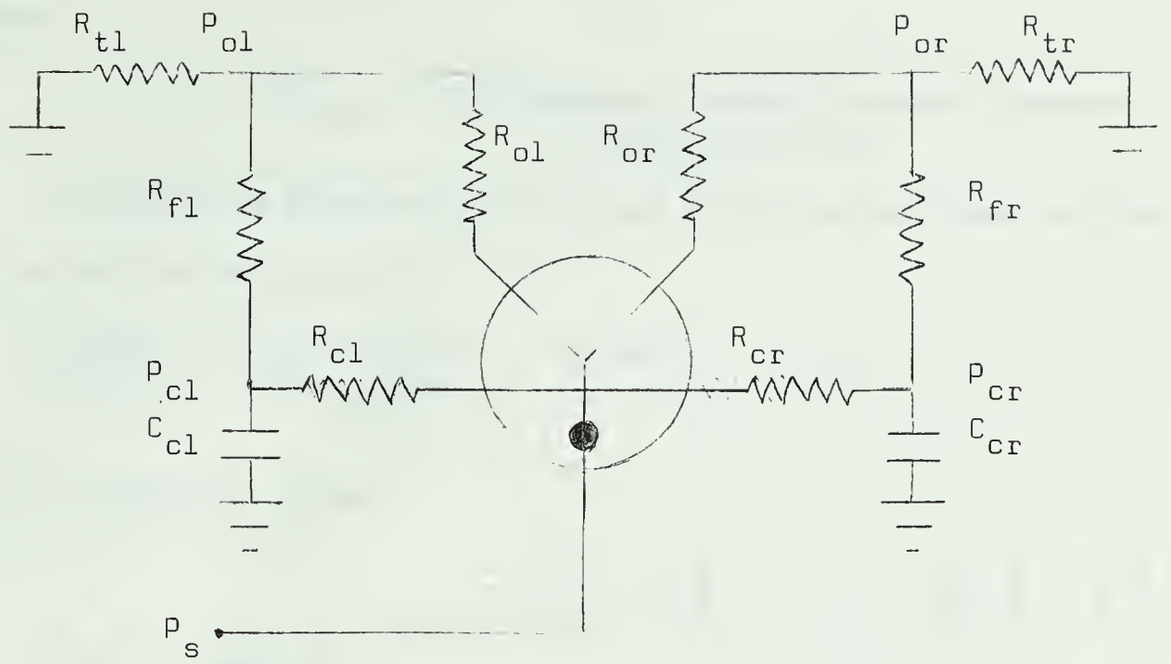
2.1 Function

Two constant frequency square wave generators are required. They operate independently. One produces the carrier signal for the Pulse Width Modulator, determining the rate at which the integrator input is sampled. A generator of higher frequency is required to provide the count input to the UP-DOWN Counter, effectively performing a digital measurement of the length of the PWM pulses.

The frequency of the high frequency generator should be approximately ten times greater than the frequency of the carrier pulses for the PWM. This results in a minimum of ripple on the output of the counter while ensuring that it responds sufficiently to small variations in the length of the PWM pulses. This is discussed further in Chapter 5. The highest frequency of square wave which could be generated was found to be 480Hz (see Appendix E) so that the maximum practical sampling frequency is 40Hz. There is no theoretical limit to the minimum frequency which can be employed, though the bulk of the components becomes excessive if frequencies too low are chosen. The frequencies chosen for the system built were 0.70Hz for the PWM carrier signal and 8.00Hz for the count input.

2.2 Square Wave Generator Circuit

The Square Wave Generator consists of an astable multivibrator with negative feedback which causes it to switch from one state to the other. The feedback path is a resistor and the input is paralleled by a capacitor. Fig. 2.1 is the equivalent circuit.



Equivalent Circuit for Square Wave Generator Fig. 2.1

The circuit operates in the following manner. If, for example, the right-hand output is ON then the pressure in the right-hand capacitor, C_{cr}, will rise, while that in the left-hand capacitor will fall until the differential control pressure is sufficient to cause the output to switch.

This circuit can be approximately analyzed using the measured performance curves, but a degree of trial and error was necessary before generators having the required performance could be built. For the purpose of this analysis the circuit is assumed symmetrical; it is also assumed that the output pressure of each leg can take one of two constant values, 0 when OFF and some positive pressure, P_o, when ON. This latter assumption is reasonable provided that R_t R_f. When the unit is performing in the steady state the control pressure at each control input varies between two limits, P_{c1} being the lower, and P_{c2} the upper.

$$P_{cds} = P_{c2} - P_{c1} \qquad (2.1)$$

where:-

P_{cds} = Differential control pressure necessary to cause switching

Writing the equation for the flow to one control port during the ON half of the cycle:-

$$\frac{P_c(s)}{R_c} + \frac{P_c(s) - P_o/s}{R_f} + sP_c(s)C_c - P_{c1}C_c = 0 \qquad (2.2)$$

which is solved to give:-

$$P_c(t) = \frac{P_o \quad R_c}{R_c + R_f} \left\{ 1 - e^{\frac{-1}{C_c}\left[\frac{1}{R_f} + \frac{1}{R_c}\right] t} \right\} + P_{c1} e^{\frac{-1}{C_c}\left[\frac{1}{R_f} + \frac{1}{R_c}\right] t} \qquad (2.3)$$

Defining the following quantities:-

$$\alpha = \frac{1}{C_c}\left[\frac{1}{R_f} + \frac{1}{R_c}\right]$$

$$\rho = \frac{P_o}{P_{cds}}$$

$$\beta = \frac{R_c}{R_c + R_f}$$

equation (2.3) may be simplified:-

$$P_c(t) = \beta P_o (1 - e^{-\alpha t}) + P_{c1} e^{-\alpha t} \qquad (2.4)$$

T is the period of the square wave.

After one half period:-

$$P_c\left(\frac{T}{2}\right) = P_{c2} = P_o\left(1 - e^{-\alpha T/2}\right) + P_{c1}e^{-\alpha T/2} \qquad (2.5)$$

By similar considerations for the OFF half of the cycle:-

$$P_{c1} = P_{c2}e^{-\alpha t} \qquad (2.6)$$

Subtracting (2.6) from (2.5):-

$$P_{cds} = \beta P_o\left(1 - e^{-\alpha T/2}\right) - P_{cds}e^{-\alpha T/2} \qquad (2.7)$$

Dividing by P_{cds}:-

$$1 = \rho\beta\left(1 - e^{-\alpha T/2}\right) - e^{-\alpha T/2} \qquad (2.8)$$

So that:-

$$T = \frac{2}{\alpha} \ln\left[\frac{\rho\beta + 1}{\rho\beta - 1}\right] \qquad (2.9)$$

Equation (2.9) indicates that T becomes infinite for:-

$$\rho\beta - 1 < 0 \qquad (2.10)$$

that is for:-

$$\frac{R_f}{R_c} > \frac{P_o}{P_{cds}} - 1 \qquad (2.11)$$

This is the expression for the maximum value of R_f which permits C_c to charge sufficiently for switching to occur. For reliable switching R_f must be chosen significantly smaller than this value. The switching frequency is then determined by C_c.

The values used in the low frequency generator were:-

P_o = 6.3 psi. R_c = 1RU

P_{cds} = 0.75 psid. R_f = 2.8RU

R_t = 2RU C_c = 0.80CU

This makes the theoretical value of T 1.36 sec. The measured value was 1.47 secs. The values chosen for the high frequency generator were:-

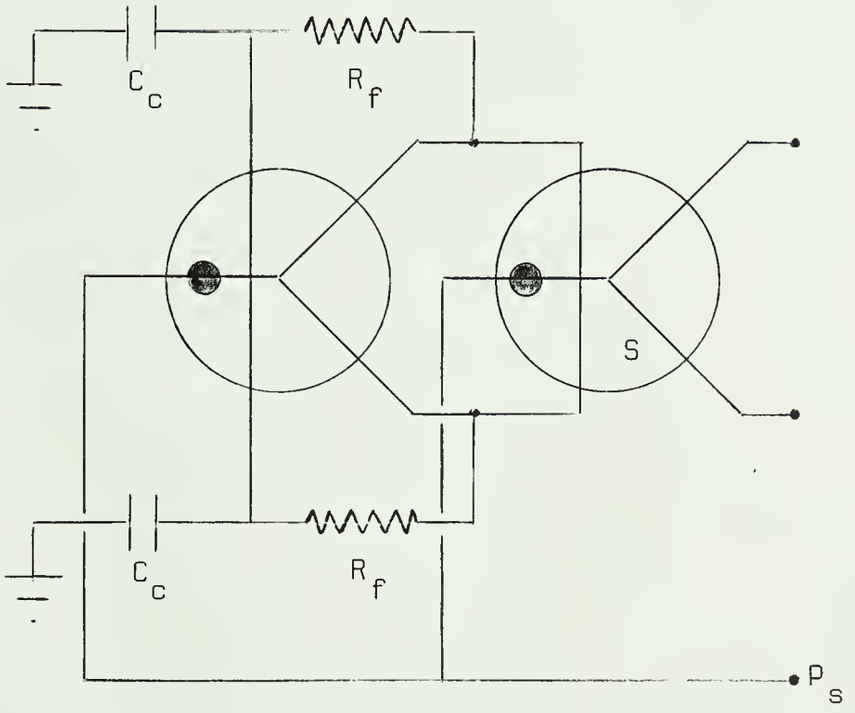
P_o = 1.7 psi. R_c = 1RU

P_{cds} = 0.35 psid. R_f = 2.2RU

R_t = 2RU C_c = 0.075CU

For this generator the theoretical value of T is 0.155 secs. The measured value was 0.125 secs.

The value of P_o is determined by the load resistance R_t, so that variation of the load will cause variation of the frequency. In order to isolate the frequency determining network from load variations it is used to switch a buffer bistable device which applies a comparatively constant load, and from which the output is taken. Fig. 2.2.



Square Wave Generator with Output Buffer Fig. 2.2

The bistable device of the basic frequency determining network must be load insensitive, in order that the frequency of switching be determined by the network and not by the instability produced by the loading. The buffer device can be load sensitive since there is always positive differential control pressure to maintain the required state irrespective of the load.

For the low frequency generator P_s was chosen as 15 psig., the maximum pressure used in the circuit. This was because the maximum possible

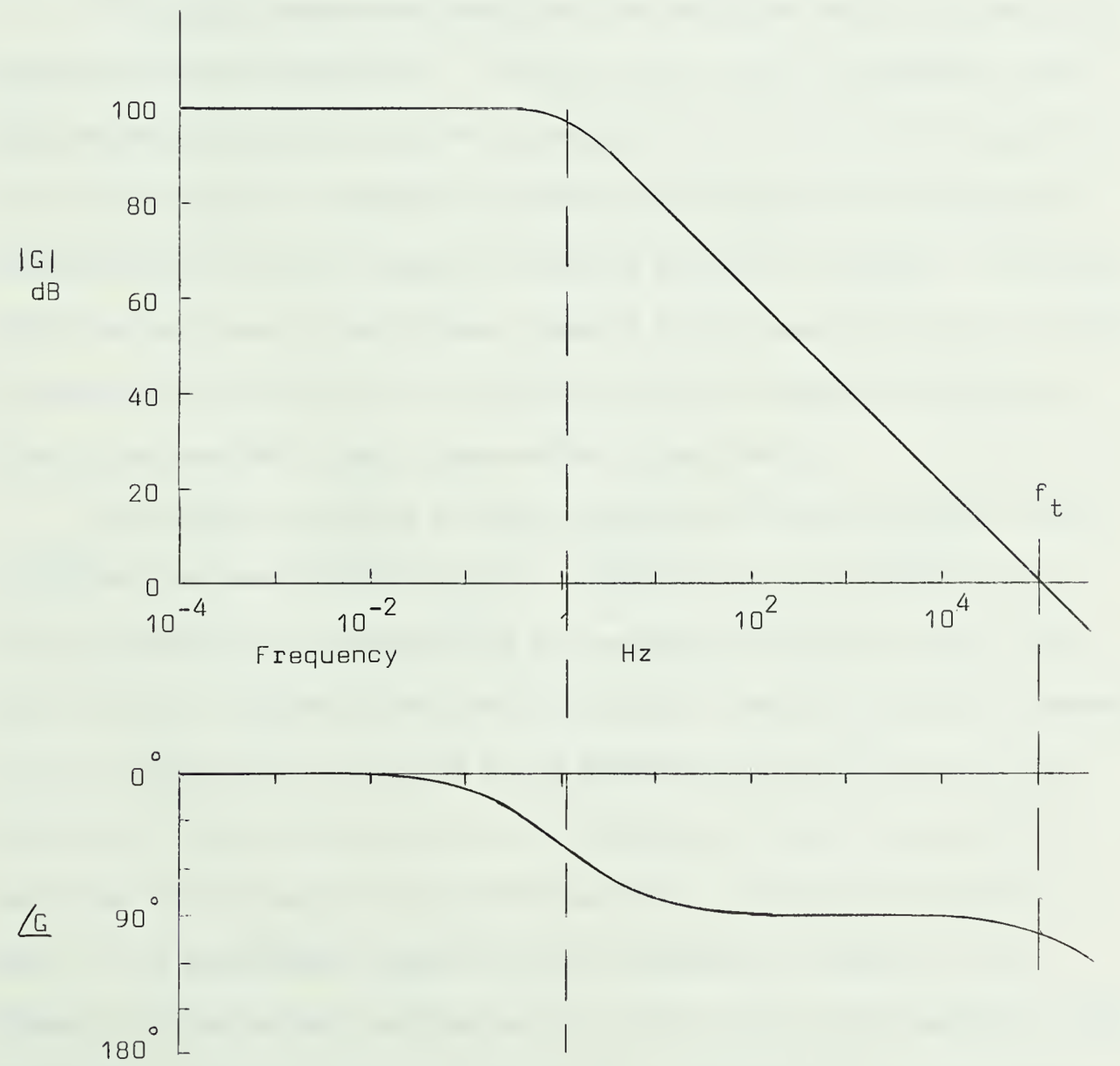
amplitude was desired. For the high frequency generator P_s was chosen to be 5 psig., this being the supply pressure used for the elements of the counter into which it feeds.

CHAPTER 3

OPERATIONAL AMPLIFIER

3.1 Function

An operational amplifier is ideally a device having high open loop D.C. gain with a uniform roll-off of 20 dB/decade at a very low corner frequency, and up to the frequency, f_t, at which the gain has fallen to one.



Ideal Open Loop Gain and Phase Characteristics of Operational Amplifier

Fig. 3.1

By the use of negative feedback round the amplifier, the gain is decreased and the bandwidth increased, the gain bandwidth product remaining constant. Although the maximum phaselag is ideally 90° additional lags are present with the result that too much negative feedback can lead to instability. The input impedance of the amplifier should normally be very high and the output impedance very low. When these conditions are met the input-output response can be made to depend only upon the passive networks which form the input and feedback paths. In particular, the relationship between input and output can be made highly linear.

A fluidic operational amplifier was designed which only partially satisfied these requirements. Its gain had a value considerably lower than the minimum which would be acceptable for an electronic amplifier. The roll-off was by no means a uniform 20dB/decade, and the phase lag exceeded 180° at a low frequency, causing stability problems. The input impedance was low. Nevertheless, despite these departures from the ideal, it was possible by the use of suitable input and feedback networks to obtain the required linear input-output relationship.

The reason for using a fluidic operational amplifier was that it permitted impedance transformation. The transfer function of a four terminal network is determined on the assumption that its input looks back into zero impedance and that its output feeds into infinite impedance. If it is required to feed into a low impedance, such as the input of an active fluidic device, then it is necessary to use an operational amplifier as an impedance transforming buffer. Because of the high gain of the operational amplifier it is necessary to feed its input through a large series resistance, R_i, which is the high impedance load required by the four terminal network. By the use of feedback resistance,

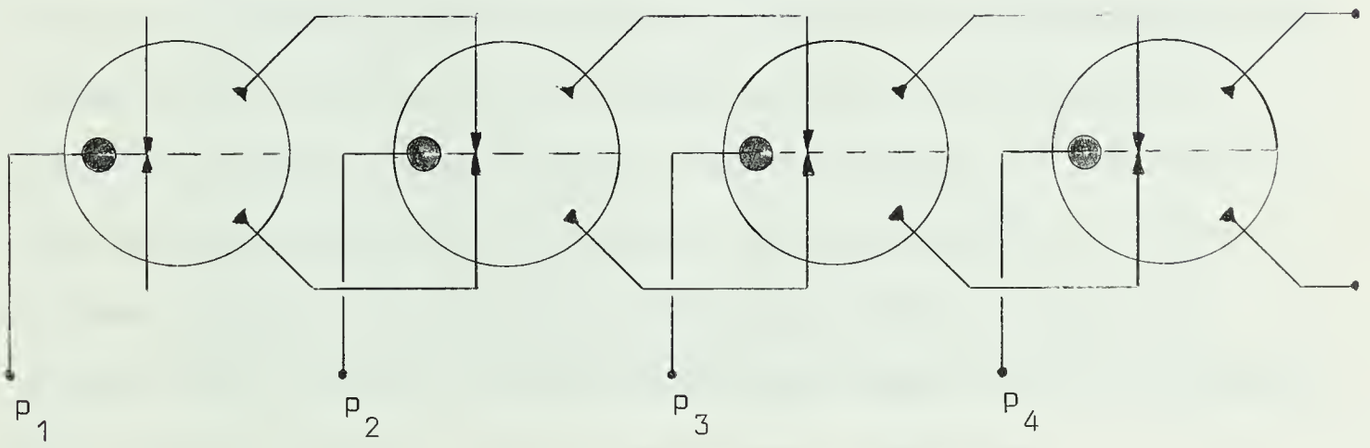
R_f, around the amplifier its output pressure is made equal to the input pressure scaled by some constant determined by the resistance values. This is true even when the amplifier is loaded by a low impedance.

To ensure that the relationship between the input pressure to R_i and the output pressure of the amplifier is linear it is important that the gain be as high as possible. This will minimize the effect of gain variations resulting from the nonlinear operation of the individual jet-deflection type proportional amplifiers used in its construction.

Operational amplifiers were employed in the Pulse Width Modulator and the Digital to Analogue Converter.

3.2 Design

The amplifier consisted essentially of four jet deflection proportional differential amplifiers in cascade, as shown by Fig. 3.2.



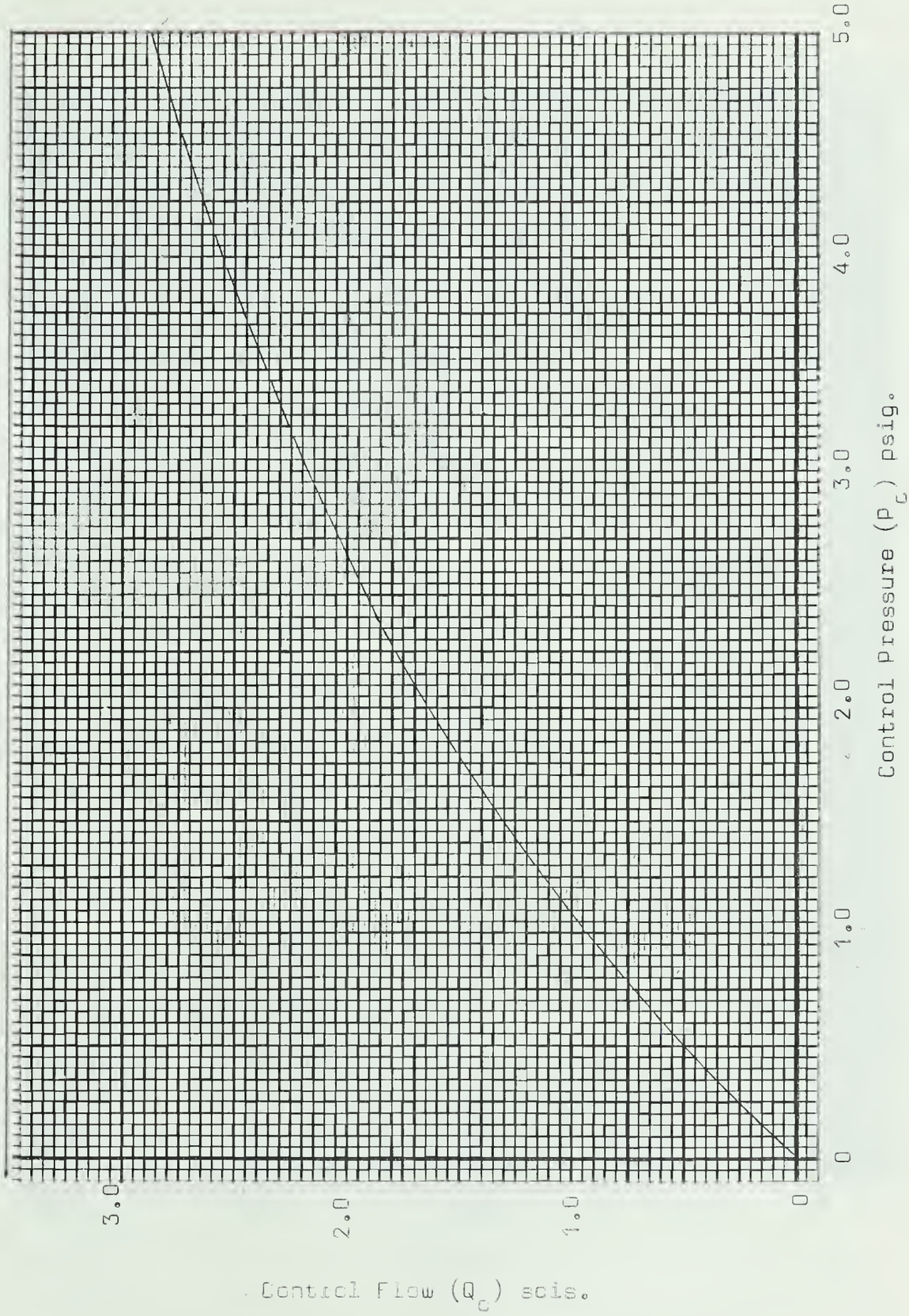
Basic Operational Amplifier Design Fig. 3.2

The design problem was the choice of type of amplifier (i.e. centre-dump or non-centre-dump) and of supply pressure for each stage. The choice

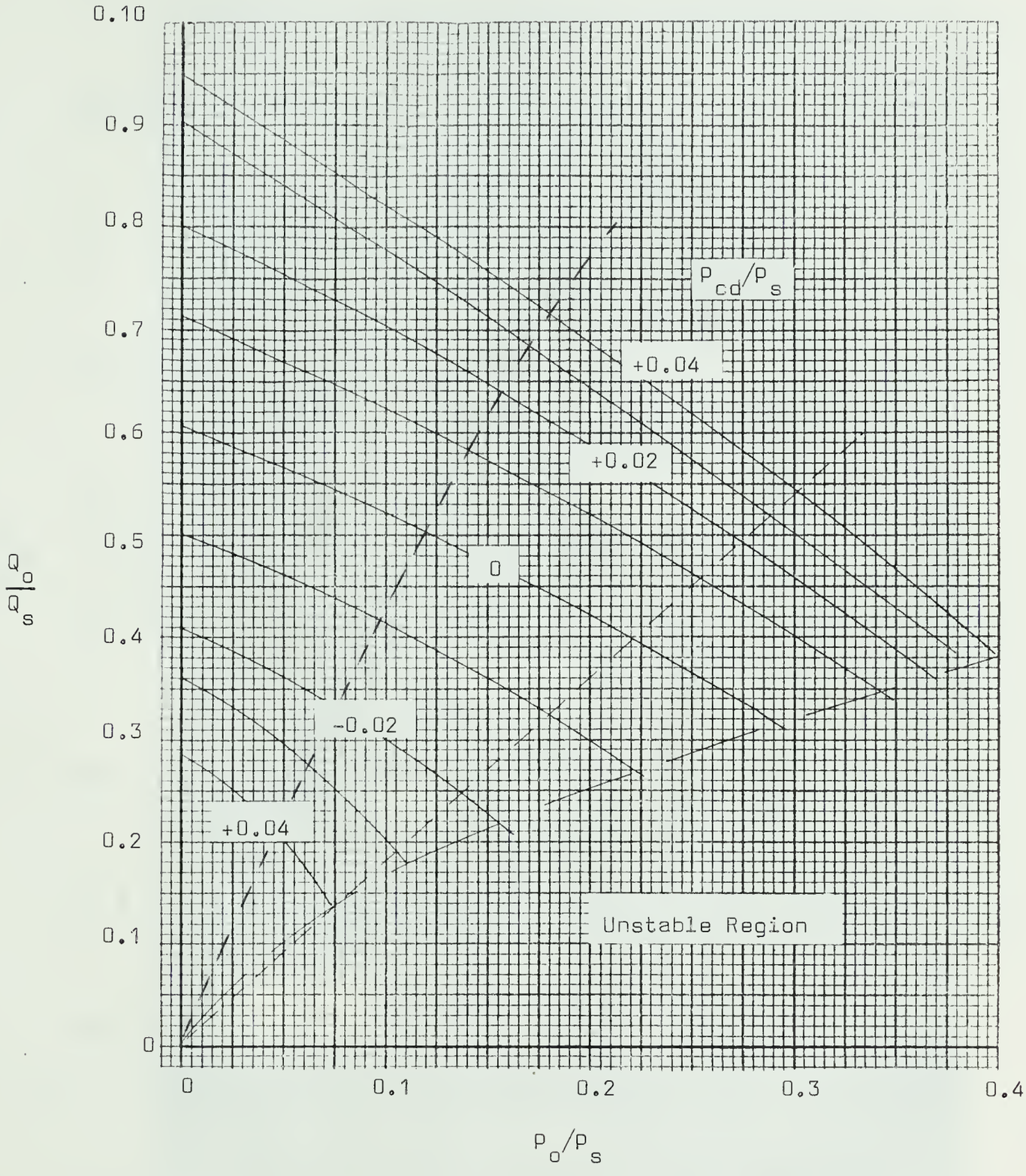
of amplifier was dictated by two conflicting requirements, gain and stability. The centre-dump amplifier has lower gain than the non-centre-dump alternative, but it remains stable under all loading conditions. The amplifier without centre-dump becomes unstable if not sufficiently loaded by the succeeding stage.

The supply pressures were chosen such that each stage is driven to saturation simultaneously if the individual stages are assumed perfectly symmetrical (Ref. 3). If supply pressures too high were chosen for the lower level stages, assymmetrical operation might result in a differential output pressure which when amplified through the succeeding stages, would drive the output stage to saturation, without any signal being present at the input. The interconnection conditions were determined by the superposition of the input characteristic (load line) of the succeeding stage upon the output characteristic of the stage under consideration, as described in References 3, 4, 5 and 6. This was done using normalized output characteristics, with supply flow and supply pressure as the normalizing factors. Although the normalized curves are not identical for all supply pressures, the variation is not great, and it is only necessary that the condition of simultaneous saturation be approximately satisfied. The characteristics of the different types of proportional amplifier are shown in Figs. 3.3 through 3.5. The output characteristics were taken with P_s of 10 psig. Fig. 3.6 is the supply curve for both types of amplifier.

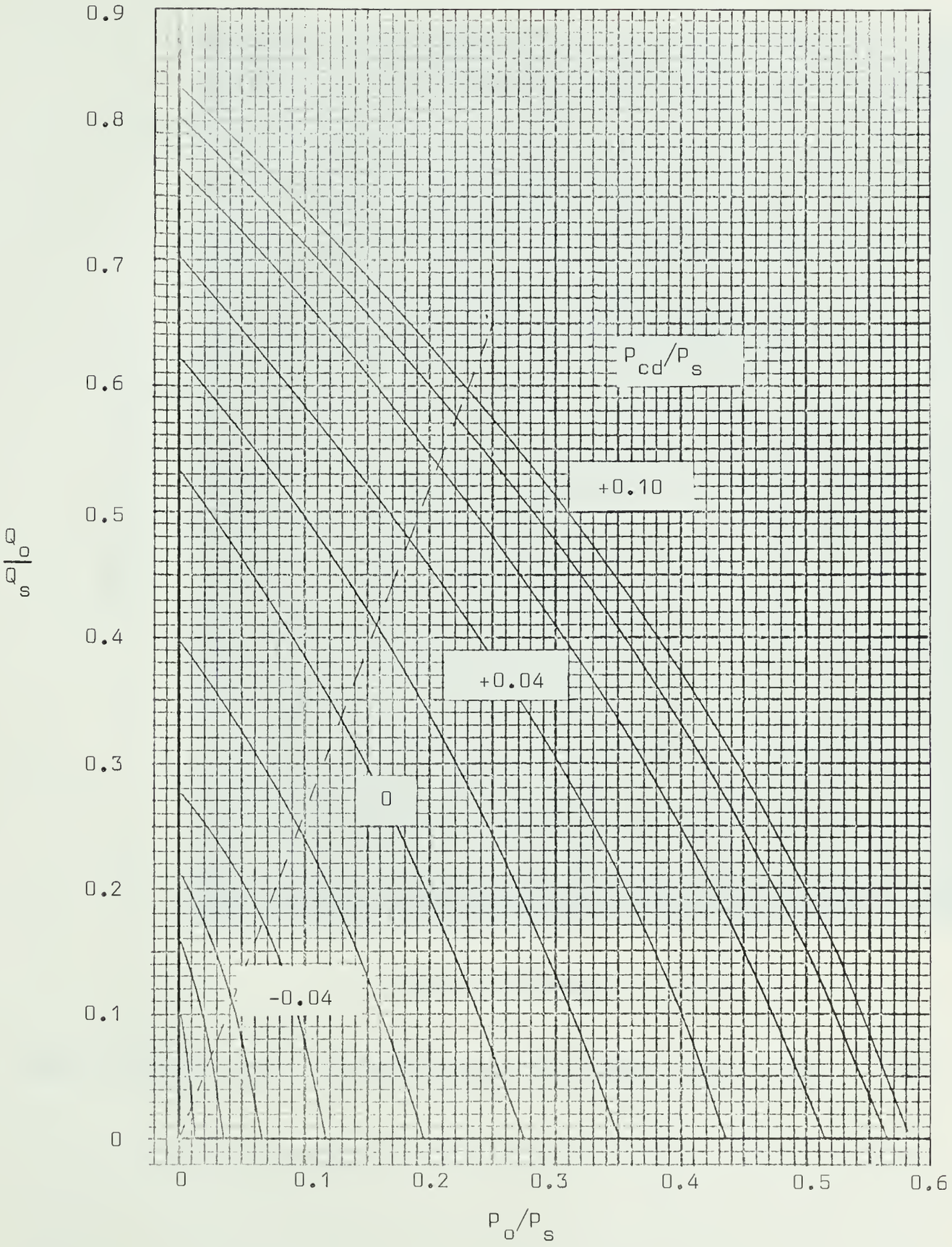
The maximum supply pressure, P_{s4}, was chosen arbitrarily as 15 psig., this being a pressure generally available from shop air lines. The design proceedure will be illustrated by the determination of the supply pressure required for the third stage, P_{s3}. The



Input Characteristic of Proportional Amplifiers (both types) Fig. 3.3

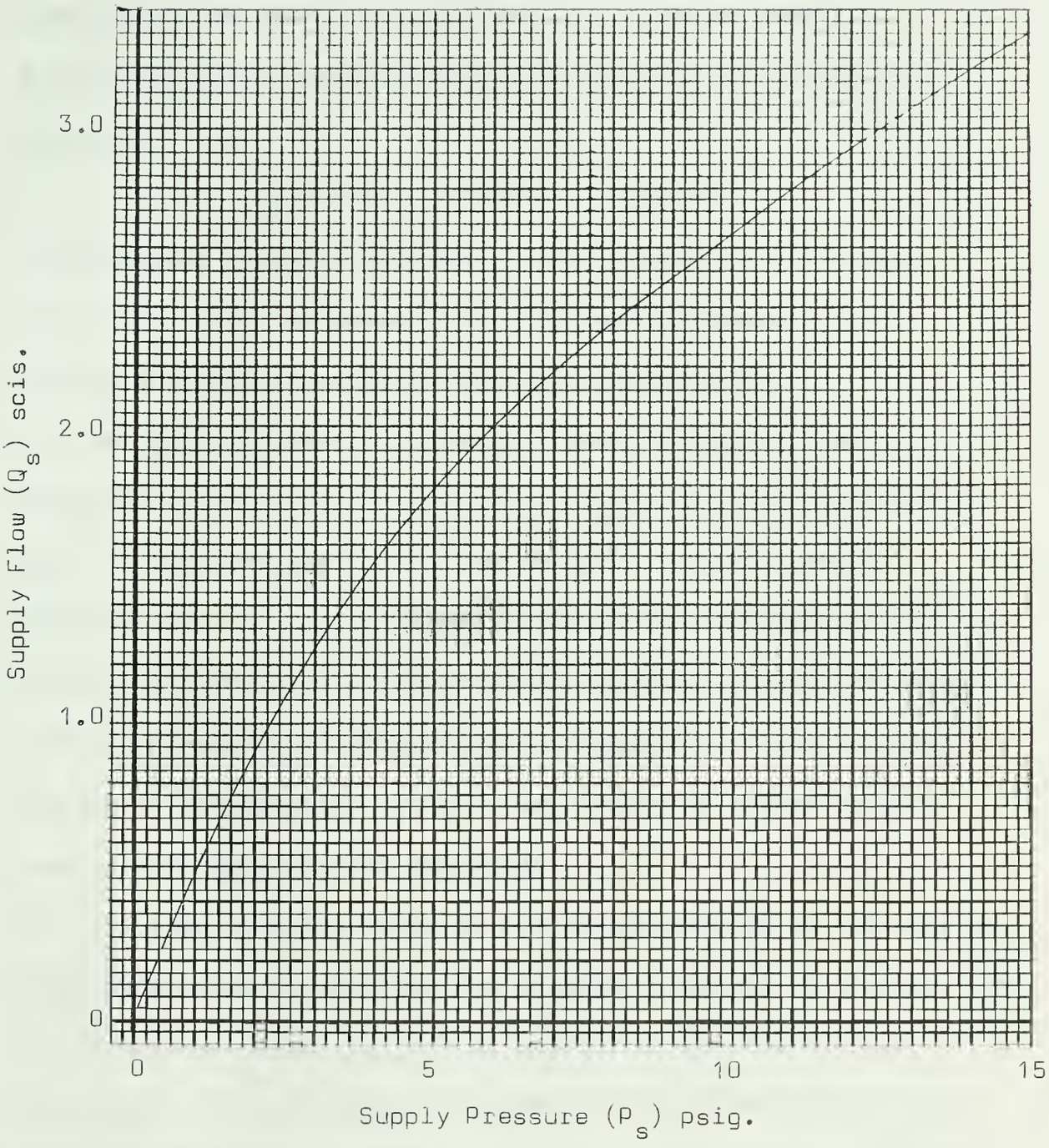


Non-Dimensionalized Output Characteristics
for Non-Centre-Dump Proportional Amplifier Fig. 3.4



Non-Dimensionalized Output Characteristics

of Centre-Dump Proportional Amplifier Fig. 3.5



Supply Characteristic of Proportional Amplifiers (both types) Fig. 3.6

steps were:-

1) Stage 4 was chosen as a non-centre-dump proportional amplifier since the loading was sufficient to ensure stability. From Fig. 3.4 the differential control pressure to cause saturation, P_{cm}, was found:-

$$P_{cm} = (0.04 \times 15)\text{psid.} = 0.6 \text{ psid.}$$

The expected load line for a one nozzle load was drawn, see Fig. 3.4. This indicated the static output pressure to be 1.8 psig. and the maximum differential gain to be 5.

2) The supply pressure for stage 3 was guessed as 3 psig., which would have been correct if the load line at this pressure were in the same position as for 15 psig. supply pressure. However, the new load line was checked on the characteristic of the non-centre-dump proportional amplifier, and it was found that it placed the operating point dangerously close to the region of instability. Stage 3 was therefore chosen to be a centre-dump proportional amplifier.

3) The load line was drawn on the characteristic of the centre-dump proportional amplifier for a supply pressure of 3 psig. The differential output pressure at saturation was found to be 0.78 psid. This is nearly the same as the differential input pressure required by Stage 4 to cause it to saturate, so that a value of the order of 3 psig. is correct for P_{s3}.

A similar proceedure was followed for Stages 1 and 2. However, it was found by experiment that although the normalized characteristic indicates instability if a non-centre-dump proportional amplifier were used for Stage 1, this did not occur. This indicates a lowering of the instability cut-off line for low supply pressures. It meant that a

non-centre-dump amplifier with its greater gain could be used. The theoretical design could only be taken as a guide; the circuit had to be optimized empirically.

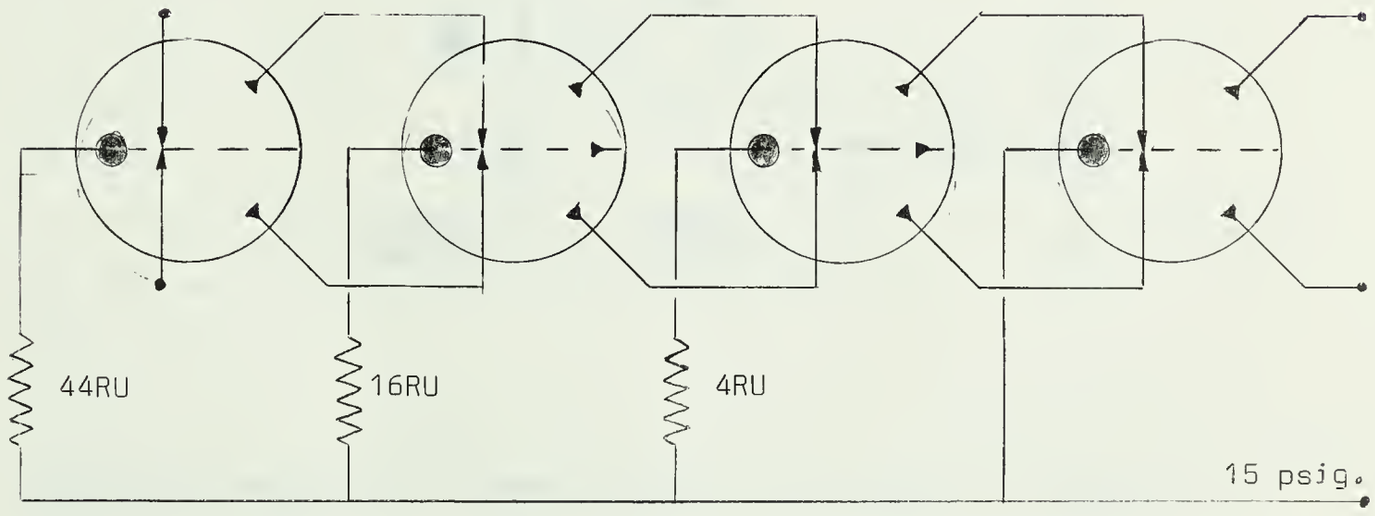
The circuit, shown in Fig.3.7 uses standard resistance values to reduce the supply pressure from the 15 psig. line value. The values of the supply pressures to each stage are:-

$$P_{s1} = 0.35 \text{ psig.}$$

$$P_{s2} = 1.6 \text{ psig.}$$

$$P_{s3} = 2.8 \text{ psig.}$$

$$P_{s4} = 15 \text{ psig.}$$



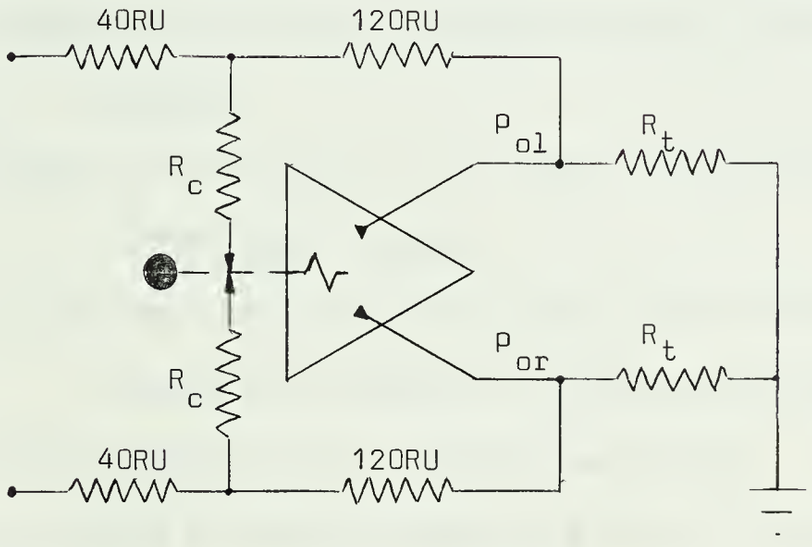
Operational Amplifier Design with Supply Pressure Bias Resistors Fig. 3.7

3.3 D. C. Performance

The D. C. gain calculated from the individual stage gains was -280. This was made on the assumption of ideal conditions, with each stage operating symmetrically, a state of affairs unlikely to be realized in practice. It did not prove possible to make open loop tests on the amplifier, due to the difficulty of applying and measuring a sufficiently low pressure signal at the differential summing junctions. From the

closed loop performance it was possible to arrive at deductions with regard to the open loop gain. For this test the amplifier was set up in the configuration shown in Fig. 3.8.

In the circuit, R_t, has a value of 1 RU, the impedance of the input nozzle of an active device. R_c has the same value. Thus the D.C. circuit equations are:-



Operational Amplifier. Closed Circuit Test Circuit. Fig. 3.8

$$\frac{P_{id} - P_{cd}}{40} + \frac{P_{od} - P_{cd}}{120} = \frac{P_{cd}}{1} \qquad (3.1)$$

$$P_{od} = AP_{cd} \qquad (3.2)$$

Where A is the open loop D.C. gain of the amplifier. The measured value of the closed circuit D.C. gain is -2, so that:-

$$P_{od} = -2P_{id} \qquad (3.3)$$

Inserting equations (3.2) and (3.3) into equation (3.1) yields a value of A of -250, a good agreement with the theory.

The single-sided output pressure range before saturation is 3.0 psi., so that the differential output pressure range is 6.0 psid.

3.4 Dynamic Characteristics

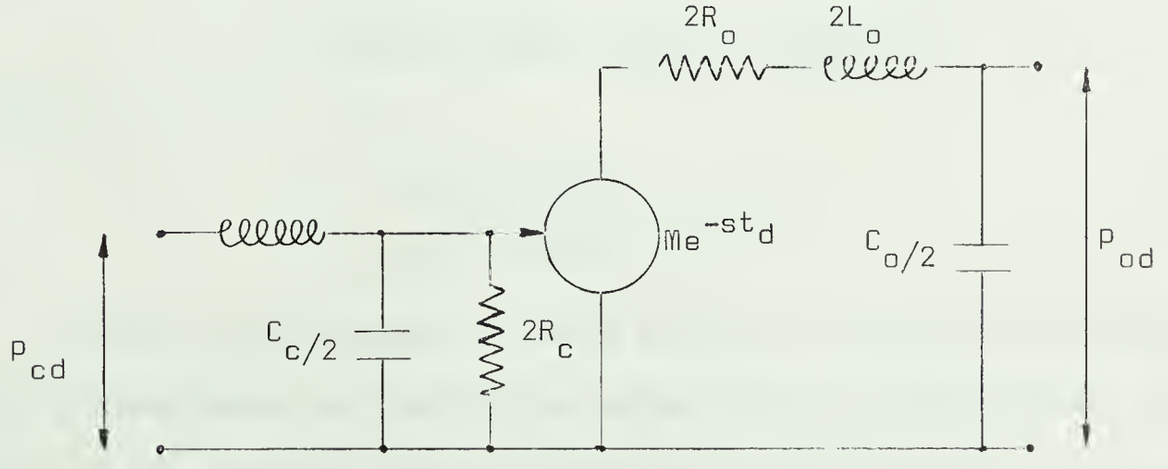
In the design of the amplifier attention was concentrated upon obtaining a high D.C. gain, since in the applications of the amplifier in this project the inputs are of a low frequency nature. The dynamic response is, however, of interest for three reasons:-

1) It determines the stability conditions when feedback is applied.

2) It affects the response of the closed loop system to sudden input changes.

3) It limits the useful frequency range of the amplifier should it be applied in other applications.

The transfer function of the amplifier was derived. Belsterling and Tsui (Refs. 4, 5 and 6) have developed an equivalent circuit for the jet deflection proportional fluid amplifier. This circuit, shown in Fig. 3.9 is the dynamic equivalent circuit for frequencies sufficiently low that standing waves are not present in the interconnecting lines.



Equivalent Circuit for Jet Deflection Proportional Amplifier Stage
Fig. 3.9

The gain of the equivalent pressure generator, M, is defined as follows:-

$$M = \left[\frac{P_{od}}{P_{cd}}\right] Q_o$$

The circuit element values can all be found to a good approximation, either from the characteristics or by measurement of the physical dimensions of the amplifier. In the case of the operational amplifier it is convenient to combine the output inductance and capacitance of one stage with the input (control port) inductance and capacitance of the succeeding stage, since both result chiefly from the interconnecting tubing.

Consider the final stage. From the output characteristic (Fig. 3.4):-

$$M = 19.00$$

$$R_o = 4.8 \text{ RU}$$

With a one nozzle load:-

$$R_t = 1 \text{ RU}$$

From the physical dimensions:-

Length of output line = 3.5 ins.

Volume of output line = 0.043 ins^3

So that:-

$$C_o = 2.9 \times 10^{-3} \text{ CU}$$

$$L_o = 3.5 \times 10^{-5} \text{ IU}$$

Clearly the inductance is small and can be neglected in comparison with the capacitance and resistance values for the frequencies of interest; that is for frequencies less than the lower corner frequency. This simplifies the equivalent circuit.

The delay time, t_d, is calculated by considering transmission of the signal through each section of the amplifier. Four separate areas need to be considered:-

1) The control input. A pressure wave is propogated through the control port, so that the delay resulting here, t_1, is given by:-

$$t_1 = \frac{\text{length of control port}}{\text{velocity of sound in the moving fluid} + \text{velocity of the fluid}}$$

2) The interaction region. The energy of the transmitting fluid is here largely kinetic, the velocity of flow being high and the pressure low. Pressure waves are insignificant, and the delay is caused by the transit time of the flowing fluid:-

$$t_2 = \frac{\text{length of interaction chamber}}{\text{velocity of fluid flow}}$$

3) The output port. Here the flow is decelerating, with kinetic energy being reconverted to pressure. Wave propogation in a moving medium is the mode of transmission:-

$$t_3 = \frac{\text{length of output port}}{\text{velocity of sound in the moving fluid} + \text{velocity of the fluid}}$$

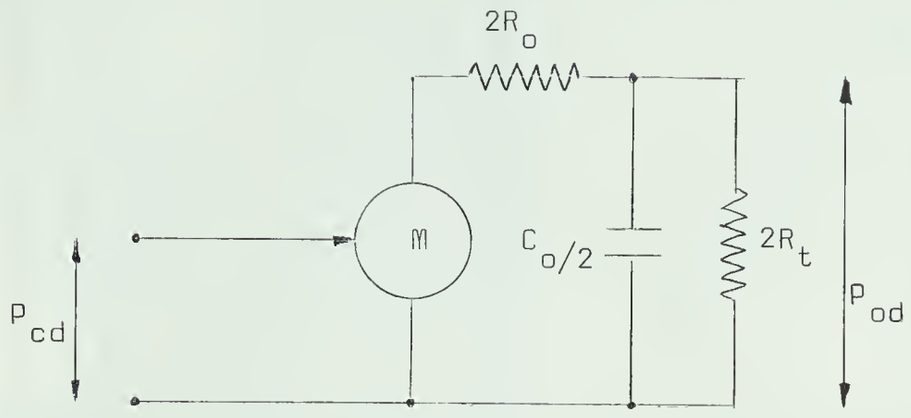
4) The output circuit. The ducts are large by comparison so that transmission of signals is essentially by wave propogation in a stationary medium:-

$$t_4 = \frac{\text{length of output duct}}{\text{velocity of sound}}$$

$$t_d = t_1 + t_2 + t_3 + t_4$$

It was assumed that the delay time is much shorter than the RC time constants, and this assumption appears to be confirmed by the measured frequency of oscillation when the loop is closed.

The simplified output circuit for the final stage is shown in Fig. 3.10.



Equivalent Circuit for Output of Final Stage Fig. 3.10

The transfer function thus becomes:-

$$\frac{P_{od}(s)}{P_{cd}(s)} = \frac{MR_t}{R_o + R_t} \quad \frac{1}{1 + \frac{sC_o R_o R_t}{R_o + R_t}} \tag{3.4}$$

Inserting known values this is:-

$$G(s) = \frac{P_{od}(s)}{P_{cd}(s)} = 5.1 \frac{1}{1 + 3.8\times10^{-3}s} \tag{3.5}$$

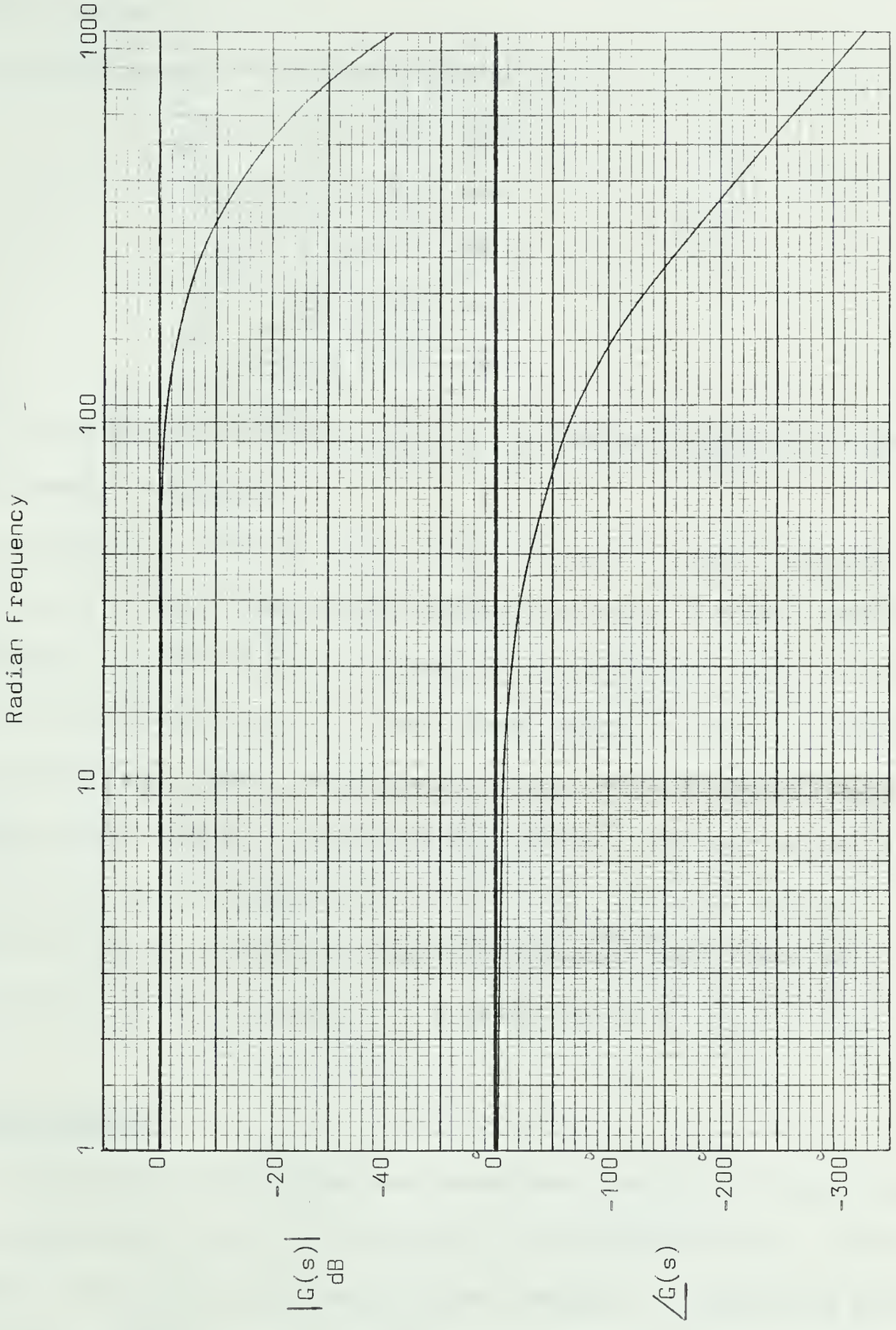
This has one corner frequency at 42Hz.

Each stage, n, of the amplifier may be treated in the same manner, and values found for M_n and T_n, the stage time constant. Account must also be taken of the input time constant of the first stage so that the overall open loop transfer function is:-

$$G(s) = M_1^{\,1} \; M_2^{\,1} \; M_3^{\,1} \; M_4^{\,1} \; \frac{1}{(1+sT_1)(1+sT_2)(1+sT_3)(1+sT_4)(1+sT_i)} \tag{3.6}$$

Where:-

$$M_n^{\,1} = \frac{M_n R_{tn}}{R_{on} + R_{t.n}} \tag{3.7}$$



Theoretical Bode Plot of Open-Loop Operational Amplifier Fig. 3.11

M_n^1 is equal to the D C. stage gain (which is the same as calculated in the static design).

The calculated value of the time constants is:-

$$T_i = 2.9 \times 10^{-3} \text{ sec.}$$

$$T_1 = 3.8 \times 10^{-3} \text{ sec.}$$

$$T_2 = 1.7 \times 10^{-3} \text{ sec.}$$

$$T_3 = 1.7 \times 10^{-3} \text{ sec.}$$

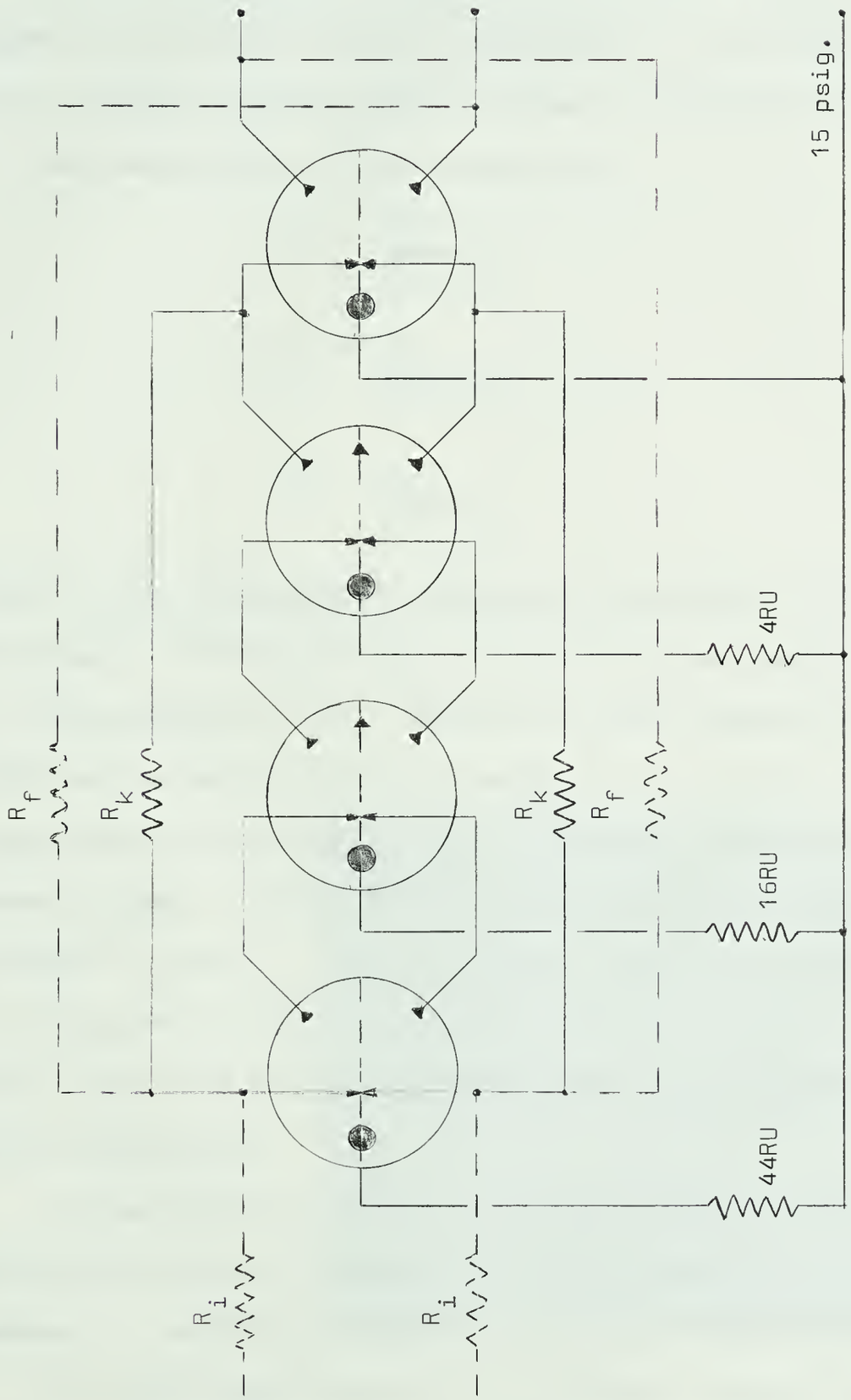
$$T_4 = 1.9 \times 10^{-3} \text{ sec.}$$

Fig. 3.11 is the resulting Bode plot for the frequency dependent terms of the transfer function.

One point of interest is the frequency at which the phase lag is 180°, as this will indicate the frequency at which the amplifier may be expected to oscillate when the feedback resistances are made sufficiently small. From the graph the point of zero phase margin occurs at a frequency of 315 radians/sec., 50Hz. With the amplifier connected as in Fig. 3.8, the value of the feedback resistances was reduced. Oscillation occured at 41.6 Hz when the resistance value was 80 RU. Since the gain is reduced by 10 dB or a factor of 3 at this frequency a D.C. gain of -240 is indicated by this value of the resistance since R_c is 1 RU.

3.5 Final Design

The minimum value of feedback resistance that could be used without further modification was found to be 80RU, as discussed above. It was found that this did not provide sufficient feedback to reduce the static output differential pressure, resulting from assymmetry of the stages, to a sufficiently low value. Additional feedback was therefore taken from the output of the third stage through resistances R_k as shown in



Operational Amplifier. Final Design. Fig. 3.12

Fig. 3.12, the final design. Here again, if R_k is chosen too small the amplifier will be unstable.

The circuit may be analyzed with the help of Fig. 3.13, the block diagram. N_1, N_2 and N_3 are the attenuations of the signals to the summing junction from the output of stage 3, the output of stage 4 and the input respectively. Their values are:-

$$N_1 = \frac{R_c}{R_k + R_c} \tag{3.8}$$

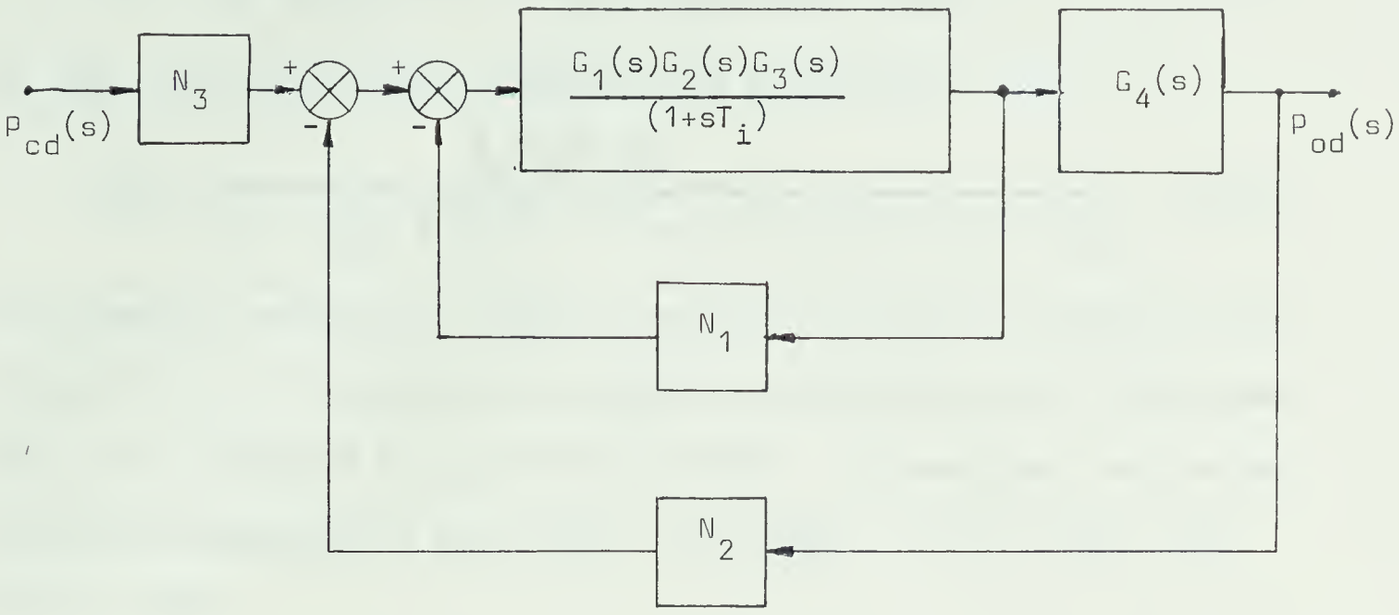
$$N_2 = \frac{R_c}{R_f + R_c} \tag{3.9}$$

$$N_3 = \frac{R_c}{R_i + R_c} \tag{3.10}$$

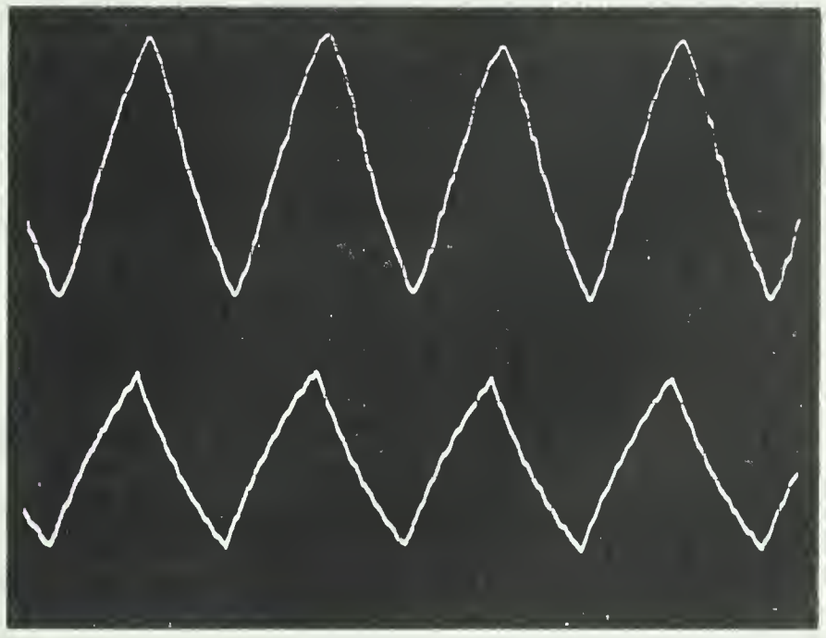
Making N_2 zero the Bode plot analysis can be applied to the feedback from stage 3. The phase margin is found to be zero degrees at a frequency of 450 radians/sec., 72Hz. Assuming the total forward loop D.C. gain to be 250 and the gain of the fourth stage to be 5 the gain of the first three stages, the product M_1^1, M_2^1, M_3^1 is 50. At 72 Hz the gain is reduced by 14dB, a factor of 5, so that the condition for sustained oscillation is that $N_1 = 1/10$, $R_k = 10RU$. It was found experimentally that sustained oscillation occurred at 93 Hz for values of R_k less than 16RU. Clearly the equivalent circuit which has been derived is only a useful approximation.

R_k was chosen to be 36RU which gave an adequate margin of stability while making possible the reduction of the static output differential pressure to a satisfactory level by choice of suitable values for R_f.

The first three stages with the feedback through R_k may now be combined into a single transfer function Q(s) where:-



Operational Amplifier. Block Diagram. Fig. 3.13



Amplifier Response to Triangular Wave. Fig. 3.14

$$Q(s) = \frac{M_1^{1} M_2^{1} M_3^{1}}{M_1^{1} M_2^{1} M_3^{1} N_1 + (1+sT_i)(1+sT_1)(1+sT_2)(1+sT_3)} \qquad (3.11)$$

so that the total forward loop gain A(s) is given by:-

$$A(s) = \frac{M_1^{1} M_2^{1} M_3^{1} M_4^{1}}{(1+sT_4)\left[M_1^{1} M_2^{1} M_3^{1} N_1 + (1+sT_i)(1+sT_1)(1+sT_2)(1+sT_3)\right]} \qquad (3.12)$$

The Bode plot analysis can again be applied to study the stability condition for N_2. It shows that a sustained oscillation at 380 radian/sec. 60Hz may be expected for N_2=1/100, R_f=100RU. The sustained oscillation measured experimentally was at 59Hz for R_f=80RU. The D.C. open loop gain is -105.

The new open loop gain of the complete amplifier was calculated from the closed loop response as 144. From this the closed loop gain of the first three stages could be deduced as 28.4. This means that the open loop gain of the first three stages must be 130, 2.6 times greater than the value before the insertion of the feedback resistors, R_k. The explanation for this is that the additional feedback is causing the individual stages to operate more symmetrically, with consequent increase in stage gain. The open loop gain of these first three stages is also now higher than that predicted theoretically. This is because the theoretical stage gains were determined taking no account of the D.C. input bias has pressure supplied by the output of the previous stage.

R_i and R_f are determined by a number of considerations. For maximum linearity and minimum static differential output pressure R_f is minimized. Together they determine the closed loop gain, and R_i is the input impedance seen by preceding circuitry. Different values of R_i and R_f were used in the two applications of this amplifier in this project.

Fig. 3.14 shows the linearity of the response obtainable. R_f was 400RU, R_i was 40RU and the input was a 4.3 Hz triangular wave with single sided amplitude of 0.65 psi. The amplitude of the output of one side was 1.95 psi.

CHAPTER 4

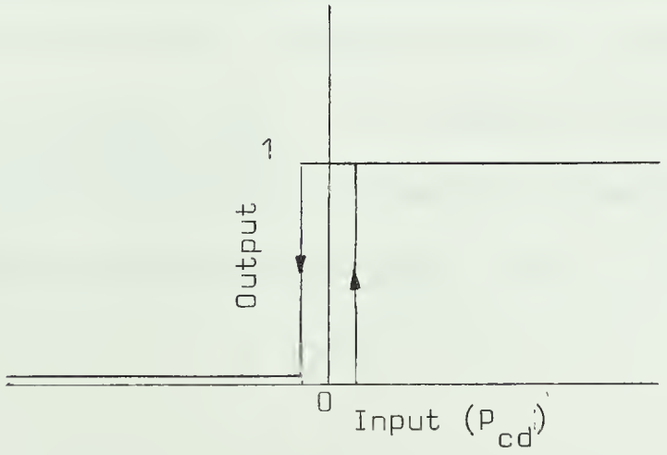
PULSE WIDTH MODULATOR

4.1 Purpose

It is required to perform the conversion of the analogue input signal to digital form with the minimum of circuitry. The method chosen was to transfer the information of the analogue signal first to a pulse width modulated carrier. The width of the pulses can then be measured digitally. This chapter describes the method of pulse width modulation.

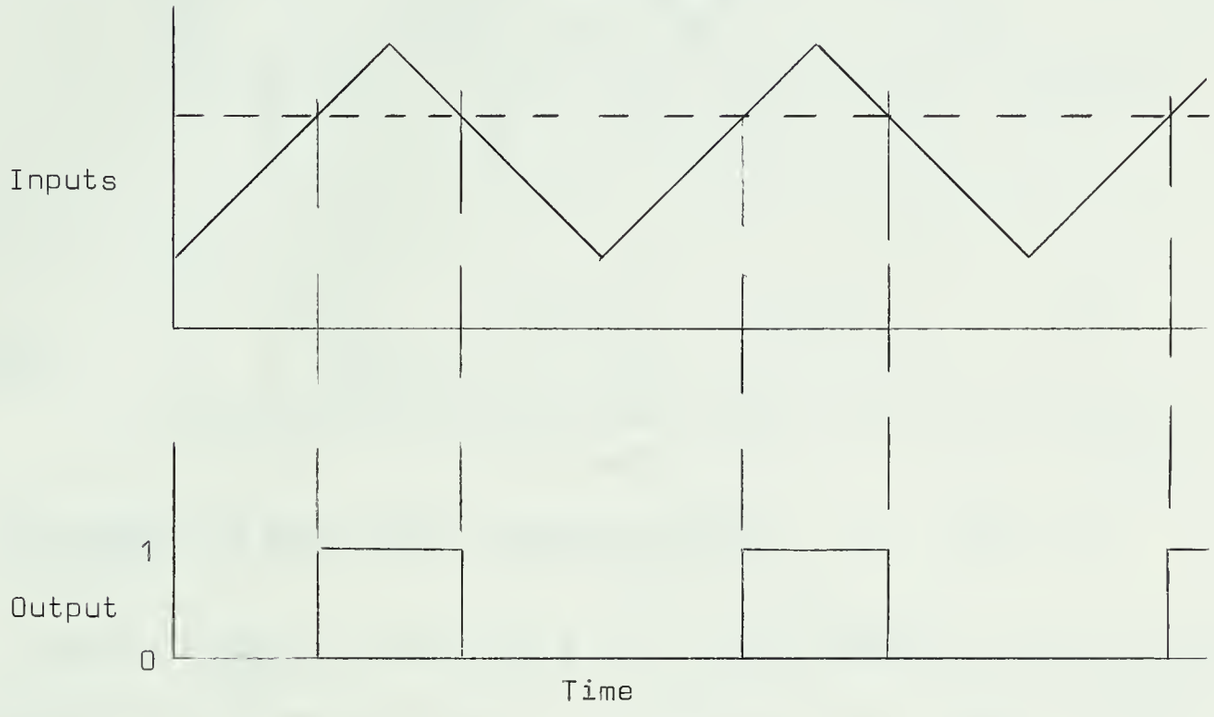
4.2 Theory of Operation

A fluidic device, the Schmitt trigger, is available which has a two-state input, governed only by the sign of the differential pressure input. Its hysteresis is minimal, so that by setting one input its output has one of two values depending upon whether the other input is above or below the threshold set by the first. See Fig. 4.1



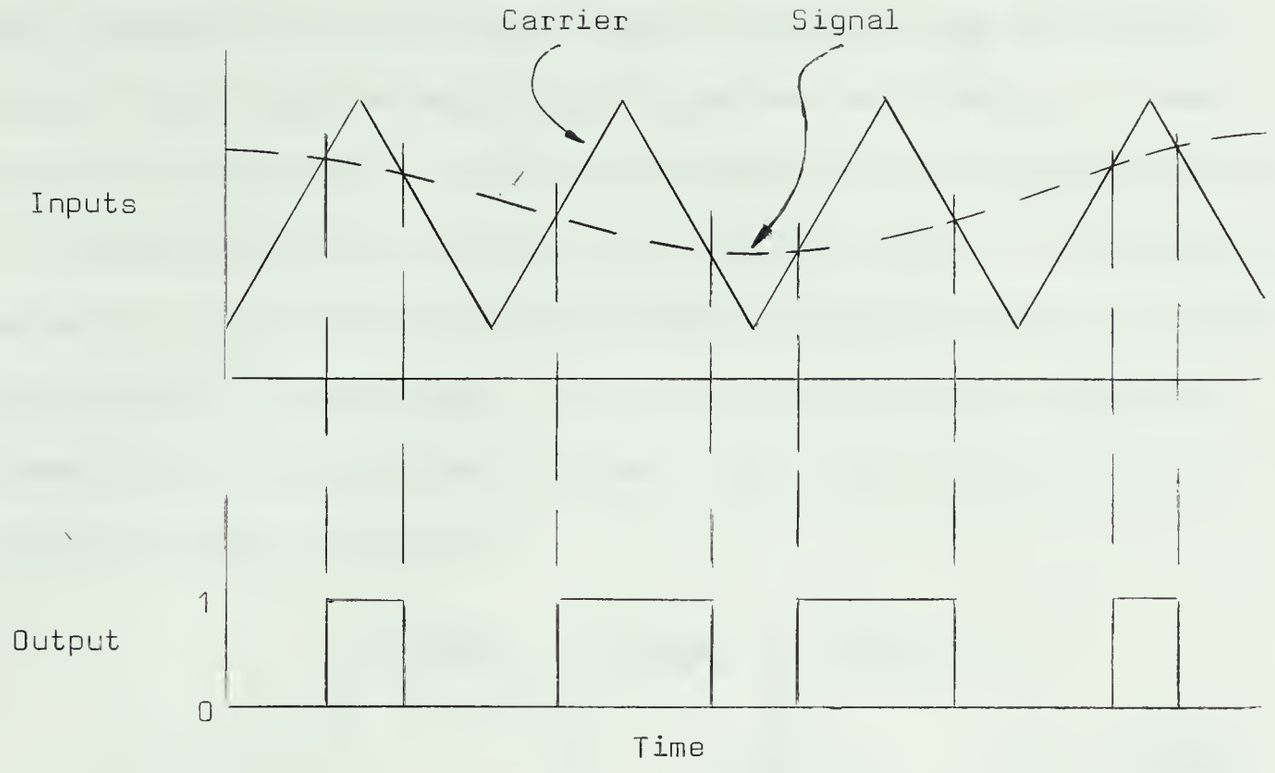
Input-Output Performance of Schmitt Trigger Fig. 4.1

If a constant signal pressure is fed to one input of a Schmitt trigger and a triangular wave is fed to the other input the trigger will change state twice during a cycle, giving a constant width pulse. (Fig. 4.2)



Constant-Width Pulse Output of Schmitt Trigger with One Input Constant, One Triangular Wave Fig. 4.2

If the constant input is now replaced by a varying signal the width of the output pulses will vary linearly with respect to the signal pressure. The output will therefore be a pulse width modulated signal carrying the information of the input signal, provided that the frequency of variation of the input is sufficiently low. By the sampling theorem it must not have a frequency more than one half the sampling frequency. In this application it should be considerably less. Fig. 4.3 illustrates the process.



Production of Pulse Width Modulated Output Fig. 4.3

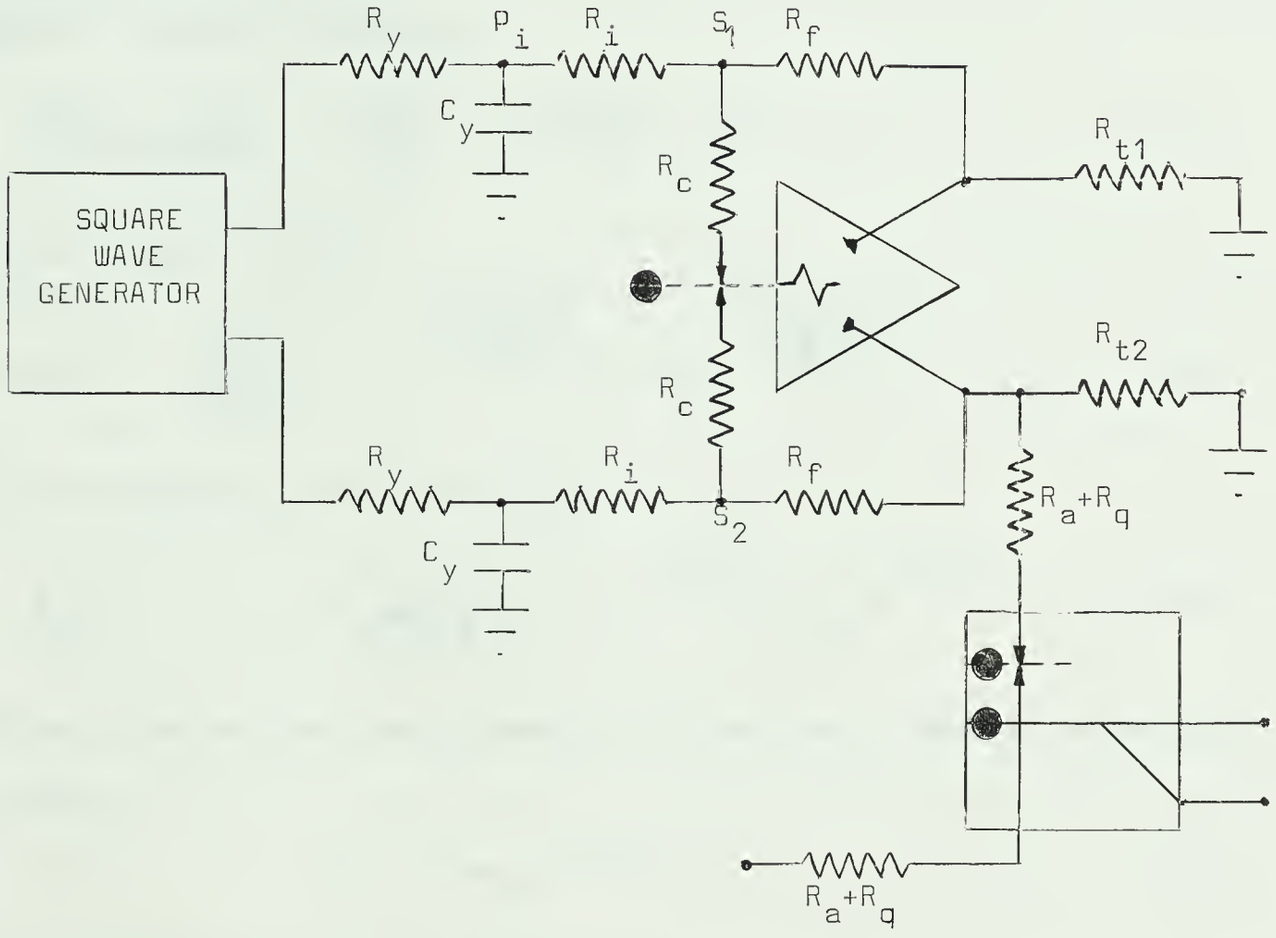
Another system for producing a pulse width modulated signal has been described by R. W. Warren (Ref. 7). This circuit was tried, but satisfactory operation could not be obtained with available components. A simulation of the system on an analogue computer was made in order to determine conditions in the network which could not be measured on the prototype. This led to the conclusion that with the parameters of the immediately available components this approach was not feasible.

4.3 Generation of Triangular Wave

A very good approximation to a triangular wave-form can be obtained by feeding a square wave into an "RC integrator," provided that the time constant of the integrator is not shorter than the ON time of the square wave.

Because of the low input impedance of the Schmitt trigger, it is necessary to use an operational amplifier as a buffer between the

R.C. integrator and the Schmitt input. In order to get the maximum output signal from the amplifier it is driven two sidedly. In other words, the differential inputs are fed from two R.C. integrators working in opposite directions, driven by the opposite outputs of the square wave generator. The maximum output variation is required which just avoids saturation of the amplifier. This and the time constant requirement determine the circuit element values. The circuit diagram for the system is shown in Fig. 4.4.



Circuit to Generate Triangular Wave Input to Schmitt Trigger Fig. 4.4

The performance of the R.C. integrators can be determined from the circuit values. The following quantities are defined:-

p_d = Amplitude of the Square Wave

p_a = Amplitude of Pressure Variation at One Input

T = Period of Square Wave

$$\alpha = \frac{(R_y + R_i)}{R_y R_i C_y}$$

P_{i1} = Minimum pressure at an input

P_{i2} = Maximum pressure at an input

The control port impedance, R_c, of the amplifier is small compared with R_i, so that points S_1 and S_2 are effectively at ground (ambient) pressure. The circuit equations may now be written for the half cycle during which the input pressure is rising:-

$$\frac{P_{i1}(s) - P_{d/s}}{R_y} + \frac{P_{i1}(s)}{R_i} + P_{i1}(s)sC - P_{i1}C = 0 \qquad (4.1)$$

This is solved to yield:-

$$P_i(t) = \frac{P_d R_i}{R_y + R_i}\left[1 - e^{\frac{-t(R_y+R_i)}{R_y R_i C_y}}\right] + P_{i1}e^{\frac{-t(R_y+R_i)}{R_y R_i C_y}} \qquad (4.2)$$

At the completion of the half cycle:-

$$P_i(t) = P_{i2} = \frac{P_d R_i}{R_y + R_i}\left[1 - e^{-\alpha T/2}\right] + P_{i1}e^{-\alpha T/2} \qquad (4.3)$$

Similarly for the half cycle during which the input pressure is falling, so that:-

$$P_{i1} = P_{i2}e^{-\alpha T/2} \qquad (4.4)$$

Adding equations (4.3) and (4.4) gives:-

$$P_a = \frac{P_d R_i}{R_y + R_i}\left[\frac{1 - e^{-\alpha T/2}}{1 + e^{-\alpha T/2}}\right] \qquad (4.5)$$

The following values were used:-

P_d = 2.85 psi
T = 1.47 sec
R_y = 12 RU
R_i = 40 RU
C_y = 0.080 CU

So that:-

$$\alpha = 1.36$$
$$\alpha T/2 = 1 = \text{ratio of half period of square wave to R.C. integrator time constant}$$
$$P_a = 1 \text{ psi}$$

The gain of the operational amplifier with R_f = 400 RU is 3, so that the amplitude of one output is 3 psi. The measured value of P_a was 0.75 psi, and that of the output amplitude was 2.25 psi, but this discrepancy could be attributed to the leakage time constant of the measuring apparatus.

4.4 Schmitt Trigger Biasing and Input Circuit

The Schmitt trigger has two supply nozzles. One provides the comparatively low pressure flow for the input amplification stage and the trigger flip-flop. The second provides the high pressure drive for the output amplification stage. These were both supplied at the maximum specified pressures for the following reasons (Appendix A):-

1) Maximum output stage supply pressure ensures sufficient output flow for the driving of subsequent devices.

2) Maximum output stage pressure also requires that the supply pressure for the input stages be set at maximum to provide sufficient drive. There is a minimum ratio between these two supply pressures of 1:3.

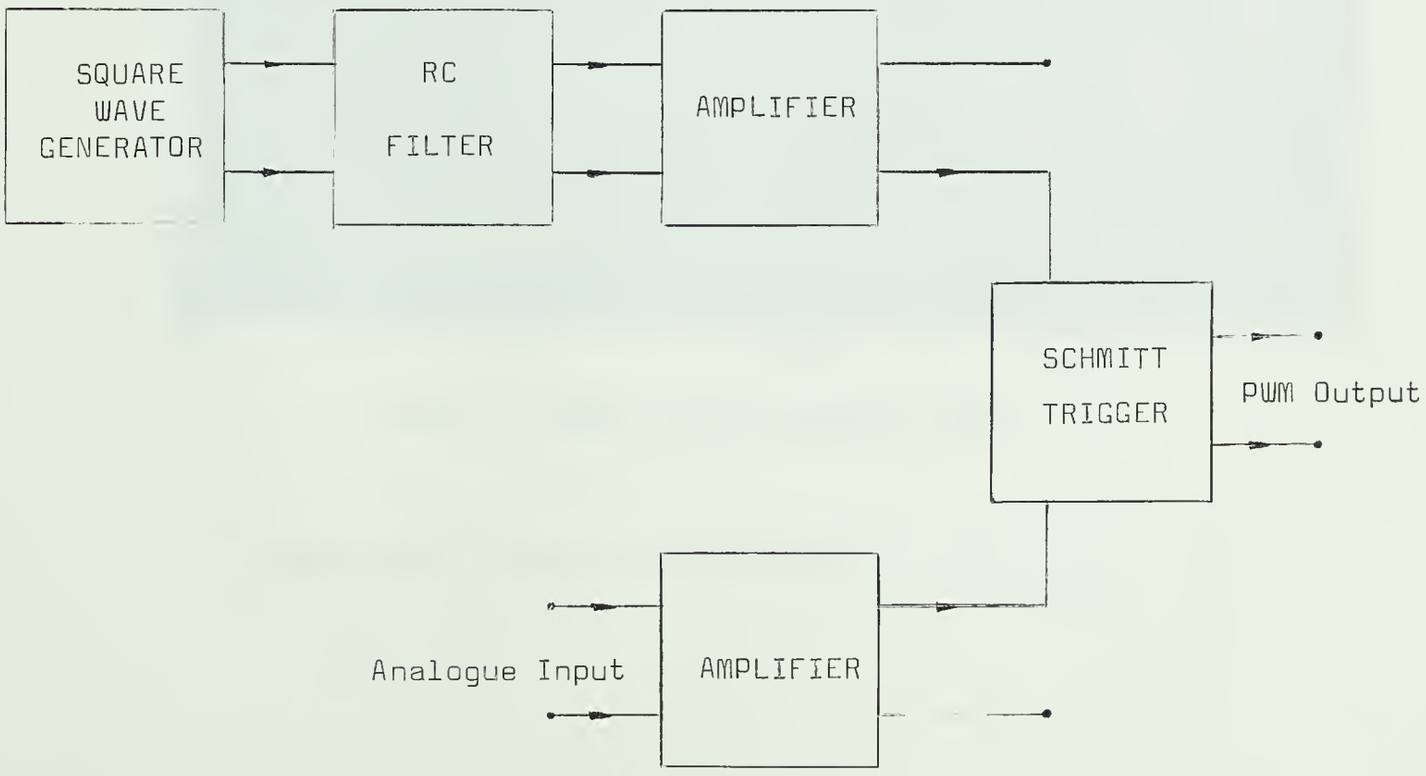
3) Use of maximum input stage supply pressure ensures that maximum input signal amplitude can be used, since this is set at 35% of input stage supply pressure. It is important for the accurate modulation of the pulse width that the time constant due to attenuating resistances between the operational amplifier output and the Schmitt trigger input be as small as possible. This means that the

signal should be attenuated as little as possible, i.e. that the largest possible signal should be fed into the trigger.

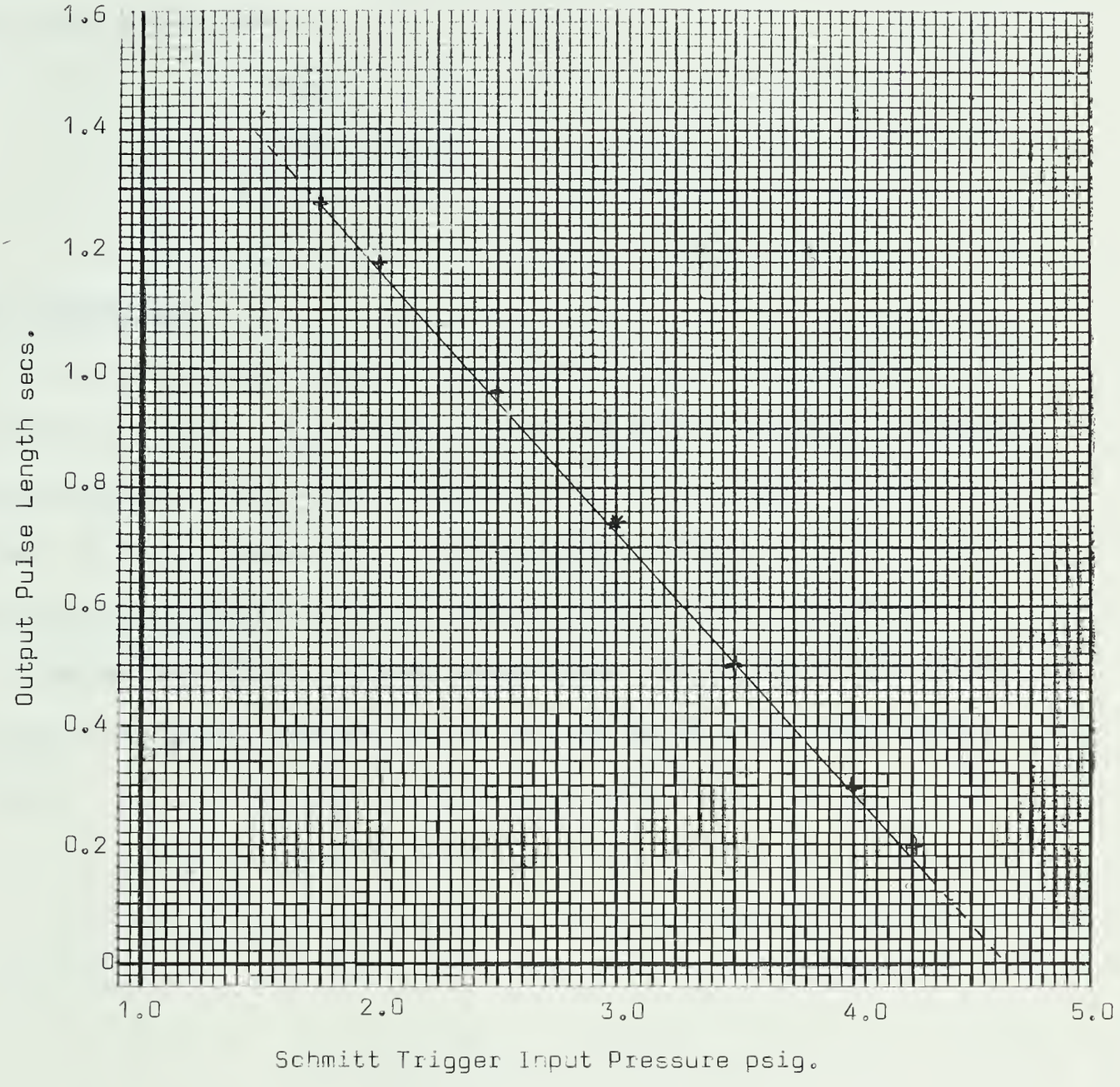
The supply pressures chosen for the trigger were therefore:-

Input stages - 2 psi
Output stage - 6 psi

An attenuating resistance R_a of magnitude 4 RU was placed in series with the input impedance R_q, of the trigger whose value is 2 RU achieving an attenuation of 1/3. This results in a theoretical maximum signal at the input of the Schmitt trigger of 1.33 psig., greater than the 0.7 psig. indicated by the specification, but not sufficient to cause erratic switching of the trigger. The switching level input signal to the Schmitt trigger is also fed through a 4 RU resistance from another amplifier, whose input sets the switching pressure. The complete PWM circuit block diagram is shown in Fig. 4.5.



Block Diagram of Pulse Width Modulation Circuit
Fig. 4.5



Pulse Width Modulator Performance Fig. 4.6

The load resistors, R_{t1} and R_{t2}, are chosen to load the final stage of the amplifier sufficiently for it to operate in its stable region. The loads on each side are balanced as closely as possible, i.e. $R_a + R_q//R_{t2} = R_{t1}$ The values chosen were:-

$$R_{t1} = 2 \quad RU$$
$$R_{t2} = 4 \quad RU$$
$$R_a + R_q//R_{t2} = 2.4 \quad RU$$

4.5 Performance

The circuit was tested for the linearity of the modulation of the width of the pulse. A pressure was applied at the alternating resistor on the variable input side of the trigger and the length of one of the output pulses was measured. The results are shown in Fig. 4.6. They show that the deviation from linearity of the output pulse time is not greater than 5% of the mean pulse time. The length of the pulses at any given input pressure varies as much as 5% of the mean pulse length.

CHAPTER 5

DIGITAL INTEGRATION

5.1 Basis of Operation

Digital integration is performed using the ON and OFF outputs of the Pulse Width Modulator to cause an UP-DOWN Counter to count in the UP and DOWN directions respectively. The counter is being driven by a pulse train of higher frequency. In effect a digital measurement is made of the length of the ON and the OFF periods. The digitalized length of the ON period is added to the counter, while that of the OFF period is subtracted.

5.2 UP-DOWN Counter

The UP-DOWN Counter was designed using the minimum number of components compatible with satisfactory operation. One important criterion was that the total in the counter should not be destroyed by a reversal of the direction of count.

The logic of the UP-DOWN counter may be expressed by the Boolean statement:-

$$C_{n+1} = P(D\overline{S}_n\overline{S_{n-1}} \ldots \overline{S}_1 + \overline{D}S_n S_{n-1} \ldots S_1) \quad (5.1)$$

C_{n+1} = Count input to $(n+1)^{st}$ stage. Count of $(n+1)$ stage changes with leading edge of C_{n+1}=1 pulse.

P = Count pulse
1 = ON; 0 = OFF

D = UP-DOWN signal
1 = UP; 0 = DOWN

S_n = Output of the n^{th} stage of the counter after change caused by C_n.

Equation (5.1) expresses the following logical requirements:-

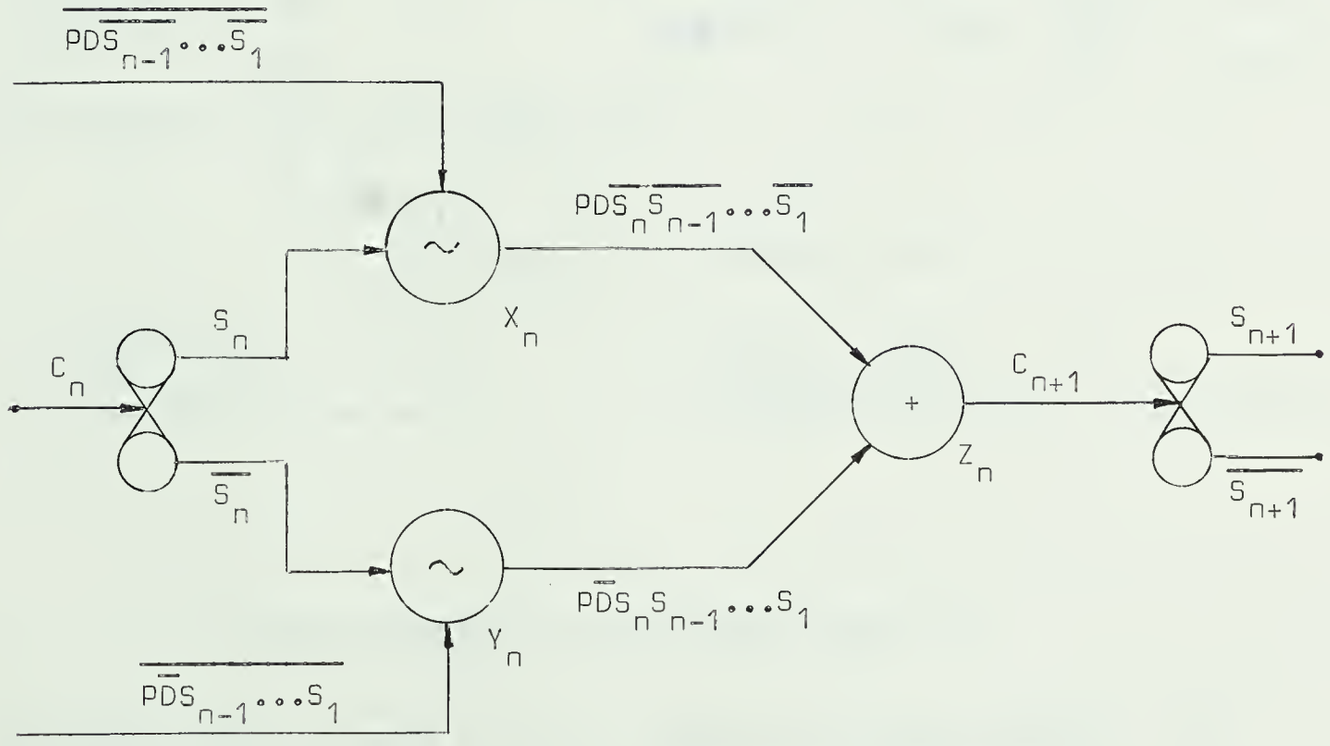
1) A carry pulse is propogated only when a count pulse is present, that is when P = 1.

2) In order for a carry to propogate to the $(n+1)^{st}$ stage, carries must also be propogated to each of the preceeding stages.

3) When the count is in the UP direction (D = 1) a carry pulse is propogated to the $(n+1)^{st}$ stage only when carries to each of the preceding stages have driven them to 0, that is $\overline{S}_n = \overline{S}_{n-1} = \ldots = \overline{S}_1 = 1$.

4) When the count is in the DOWN direction ($\overline{D}$ = 1) a carry pulse is propogated to the $(n+1)^{st}$ stage only when carries to the preceding stages have driven them to 1, that is $S_n = S_{n-1} = \ldots = S_1 = 1$.

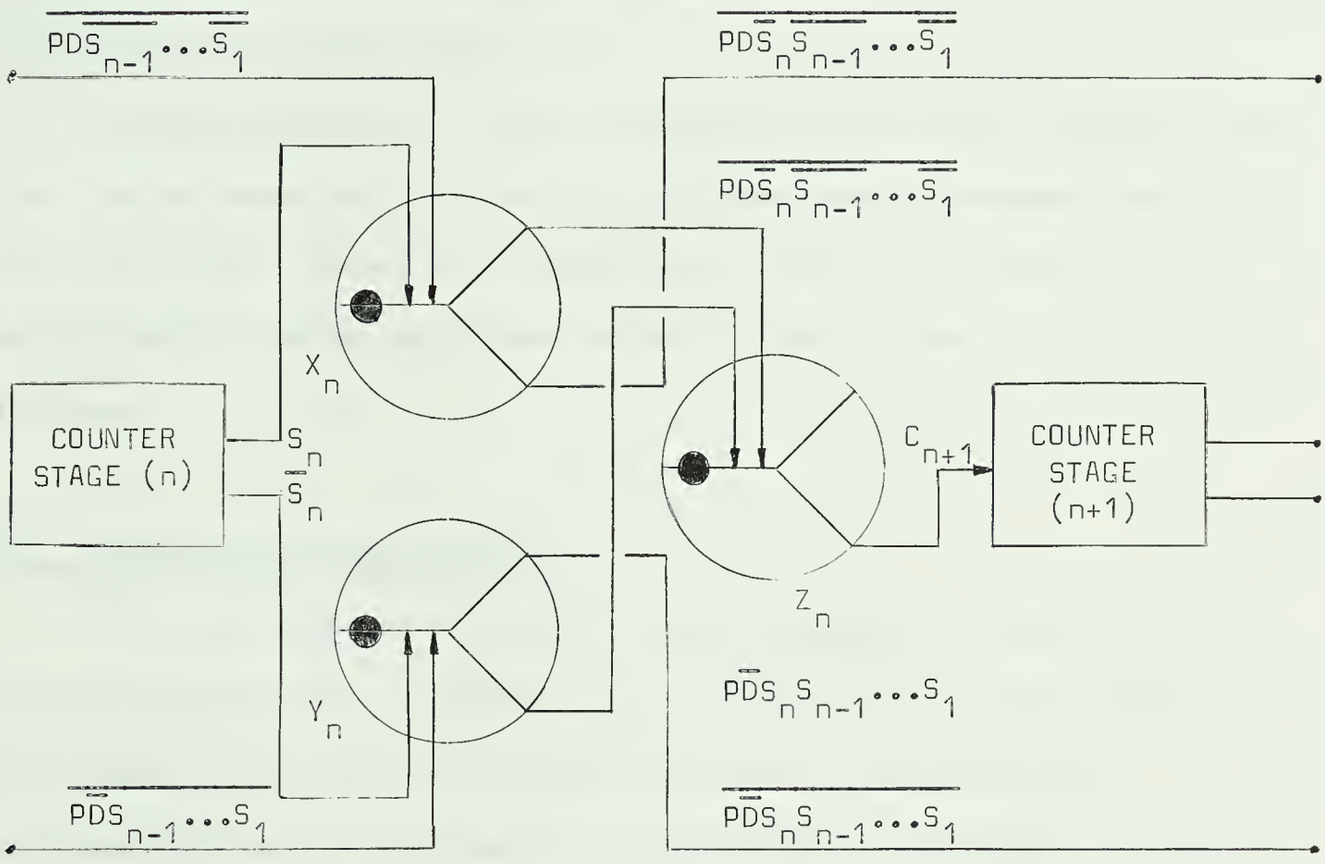
The implementation of the logical function by means of logic gates and toggle flip-flops is illustrated by Fig. 5.1.



Logic Gate Implementation of UP-DOWN Counter Fig. 5.1

As can be seen, if the inputs to gate X_n are S_n and $\overline{PDS_{n-1}\cdots S_1}$ then the output is $PDS_{n-1}\cdots S_1$, and similarly for gate Y_n. The input $\overline{PDS_{n-1}\cdots S_1}$ is available as the inverse of the output of gate X_{n-1}. Gate X_o generates the output PD from $\overline{P}$ and $\overline{D}$, while gate Y_o generates $P\overline{D}$.

The fluidic circuit can now be designed from the logic diagram. Fig. 5.2 is the result.



Fluidic UP-DOWN Counter Circuit. Fig. 5.2

The NOR outputs of gates X_n and Y_n produce the signals $P\overline{DS_n}\,\overline{S_{n-1}\cdots S_1}$ and $P\overline{DS_n}\,S_{n-1}\cdots S_1$, which generate the carry C_{n+1}; the OR outputs produce the inverses of these signals needed as inputs to the next stage.

Gates X_n and Y_n normally have the OR output ON, since the inputs from

the gates X_{n-1} and Y_{n-1} are normally ON. For a carry signal to be produced one of these inputs must go OFF and S_n must be in the correct state. A carry will also have gone to stage n; the state of S_n which applies is the state after this carry. It is important that the input to gate X_n or Y_n from the gate X_{n-1} or Y_{n-1} should not change from ON to OFF before S_n has changed state; otherwise a false carry pulse may be produced. To ensure this condition is satisfied the input to X_n or Y_n from X_{n-1} and Y_{n-1} is delayed 1 m sec by the use of 12 inches of tubing, which forms a pneumatic delay line.

A supply pressure of 5 psig. is used for the X and Y gates and also the counter elements, this being the minimum supply pressure specified for the counter. Gates Z are supplied at 8 psig., in order that the output should provide sufficient drive for the counter to function reliably.

5.3 Theoretical Considerations

It is necessary to prove that this arrangement of counting UP during the ON period of the PWM wave and DOWN during the OFF period does cause the output of the counter to have a numerical value corresponding to the integral of the signal fed to the PWM. A number of simplifying assumptions are made:-

1) The period of the PWM wave is T; the period of the count pulses is aT where $\frac{1}{a} = n$, n being an integer.

2) The average ON time of the PWM wave is bT, so that the average OFF time is (1-b)T.

3) $bT/a = m_1 + \delta_1$ where m_1 is an integer and δ_1 is a positive increment less than one; $(1-b)T/a = m_2 + \delta_2$, similarly.

$\delta_1 + \delta_2 = 1$; $m_1 + m_2 + \delta_1 + \delta_2 = n$.

4) The actual ON time during a specific sample period is $(b+\epsilon)T$, where ϵ can take any value in the range $-\frac{aT}{2}$ to $+\frac{aT}{2}$; each of the values within this range has an equal probability of occurring.

5) The ON pulse and the UP count pulse go on simultaneously. Also since P is used to count UP and $\overline{P}$ to count DOWN, the OFF pulse and the DOWN count pulse go off simultaneously.

If n_1 is the number of UP count pulses and n_2 is the number of DOWN count pulses, during one sample period, then for $\delta_1 > 1/2$:-

Probability that $n_1 = (m_1 + 2)$ is $(\delta_1 - 0.5)$ (5.2)

Probability that $n_1 = (m_1 + 1)$ is $(1.5 - \delta_1)$ (5.3)

Probability that $n_2 = m_2$ is $(\delta_1 - 0.5)$ (5.4)

Probability that $n_2 = (m_2 + 1)$ is $(1.5 - \delta_1)$ (5.5)

Then the most probable output after p sample periods, where p is a sufficiently large number, N_p, is given by:-

$$N_p = (\overline{m_1 + 2} - m_2)(\delta_1 - 0.5)n + (\overline{m_1 + 1} - \overline{m_2 + 1})(1.5 - \delta_1)n \quad (5.6)$$

$$= (m_1 - m_2)n + (2\delta_1 - 1)n \quad (5.7)$$

which is the length that N_p should have if the integration is ideal. A similar argument applies for $\delta_1 < 1/2$.

It is the variation, ϵ, or jitter in the value of the ON and OFF pulse times which makes possible the integration when the average difference between these pulse times is less than the length of one count pulse; that is when $m_1 = m_2$ and $(2\delta_1 - 1) < 1$.

In the actual system the PWM period is not an exact multiple of the count pulse period. Also ϵ has a Gaussian distribution. The argument

above can be extended to account for this departure from the assumptions made. The standard deviation of ϵ should be at least aT/2. Since it was found that the variation of ϵ was at least 5% of the PWM period the maximum value of a can be determined:-

$$\frac{1}{20} T > \frac{aT}{2} \qquad (5.8)$$

$$a < 0.1 \qquad (5.9)$$

This means that the count pulse frequency should be at least ten times greater than the PWM frequency. Because ϵ has a Gaussian probability distribution the gain of the integrator will not be the same for small inputs where $m_1=m_2$ and $(2\delta_1 - 1) < 1$ as for large inputs where $m_1-m_2 > 0$.

In order to accommodate positive and negative integrals the counter is preset with the most significant digit at 1 and each of the other digits at 0. This is the mean output of the counter; positive integrals will be outputs greater than the mean, and negative integrals will be less than the mean. The Digital to Analogue Counter is set to give zero output when the counter is preset.

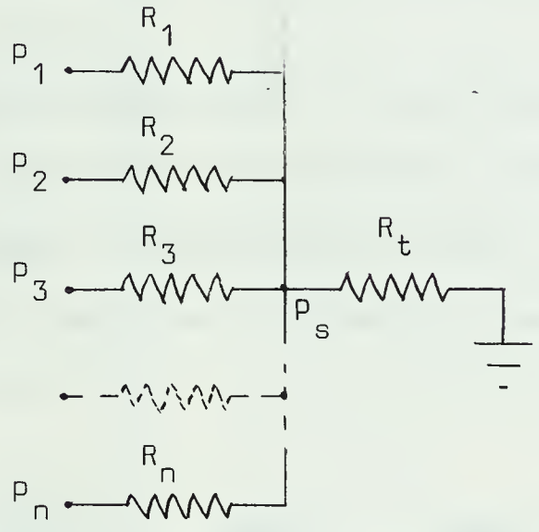
If an input to the integrator persists for too long the counter will run over range, starting again at the opposite end of the range. In order to prevent this occurring the UP count pulses must be inhibited when it reaches the top end of the range, and the DOWN pulses inhibited at the bottom end. This can be done either by sensing and combining by means of gates the output of each individual stage, or the output of the Digital to Analogue Converter can be sensed by means of Schmitt triggers, which send inhibit pulses to gates through which the P and $\overline{P}$ pulses must pass before entering the X_o and Y_o gates.

CHAPTER 6

DIGITAL TO ANALOGUE CONVERSION

6.1 Circuit Design

The basis of the digital to analogue converter is the circuit illustrated in Fig. 6.1.



Basis of Circuit of Digital to Analogue Converter Fig. 6.1

The following relationship holds for this circuit:-

$$P_s\left[\frac{1}{R_t} + \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots \frac{1}{R_n}\right] = \frac{P_1}{R_1} + \frac{P_2}{R_2} + \frac{P_3}{R_3} + \cdots \frac{P_n}{R_n} \qquad (6.1)$$

which may be expressed as:-

$$KP_s = \frac{P_1}{R_1} + \frac{P_2}{R_2} + \frac{P_3}{R_3} + \cdots \frac{P_n}{R_n} \qquad (6.2)$$

Clearly, P_s is the sum of terms each of which is proportional to one of the supply pressures and inversely proportional to its associated

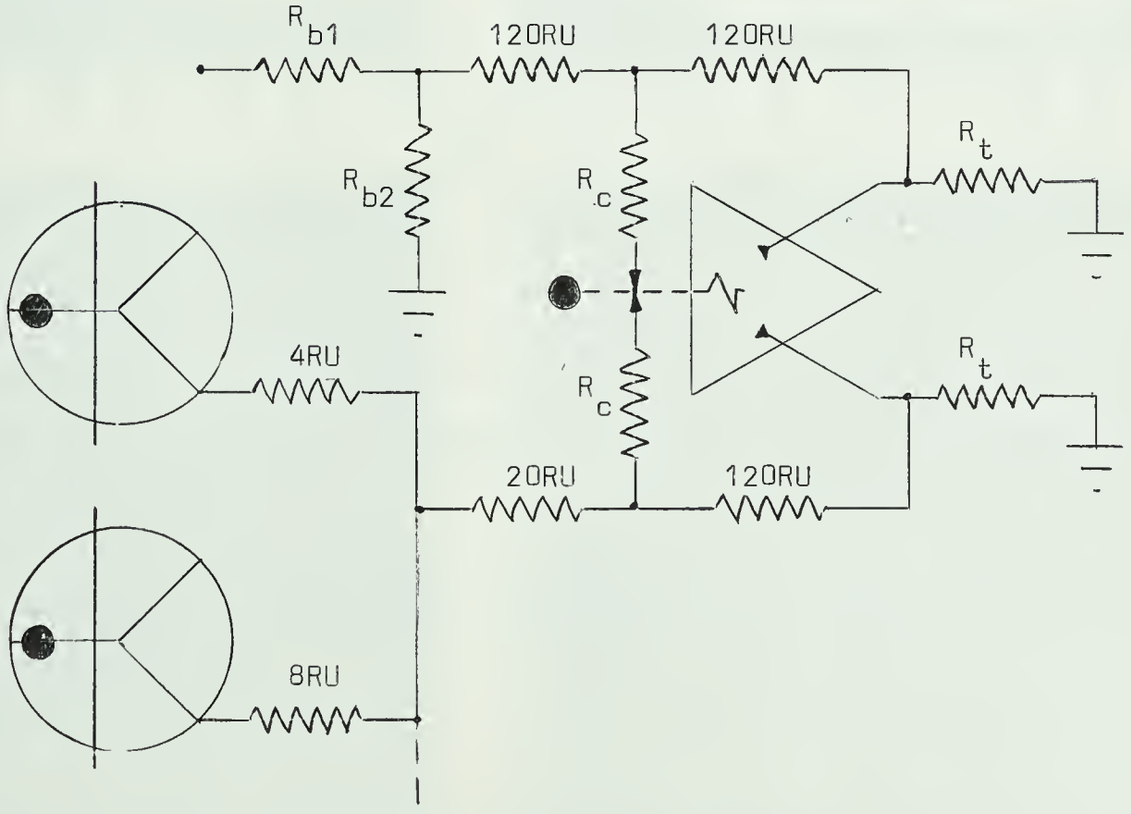
resistance. This circuit performs binary digital to analogue conversion under the following conditions:-

1) Each of the inputs can be zero or some positive pressure, P_i

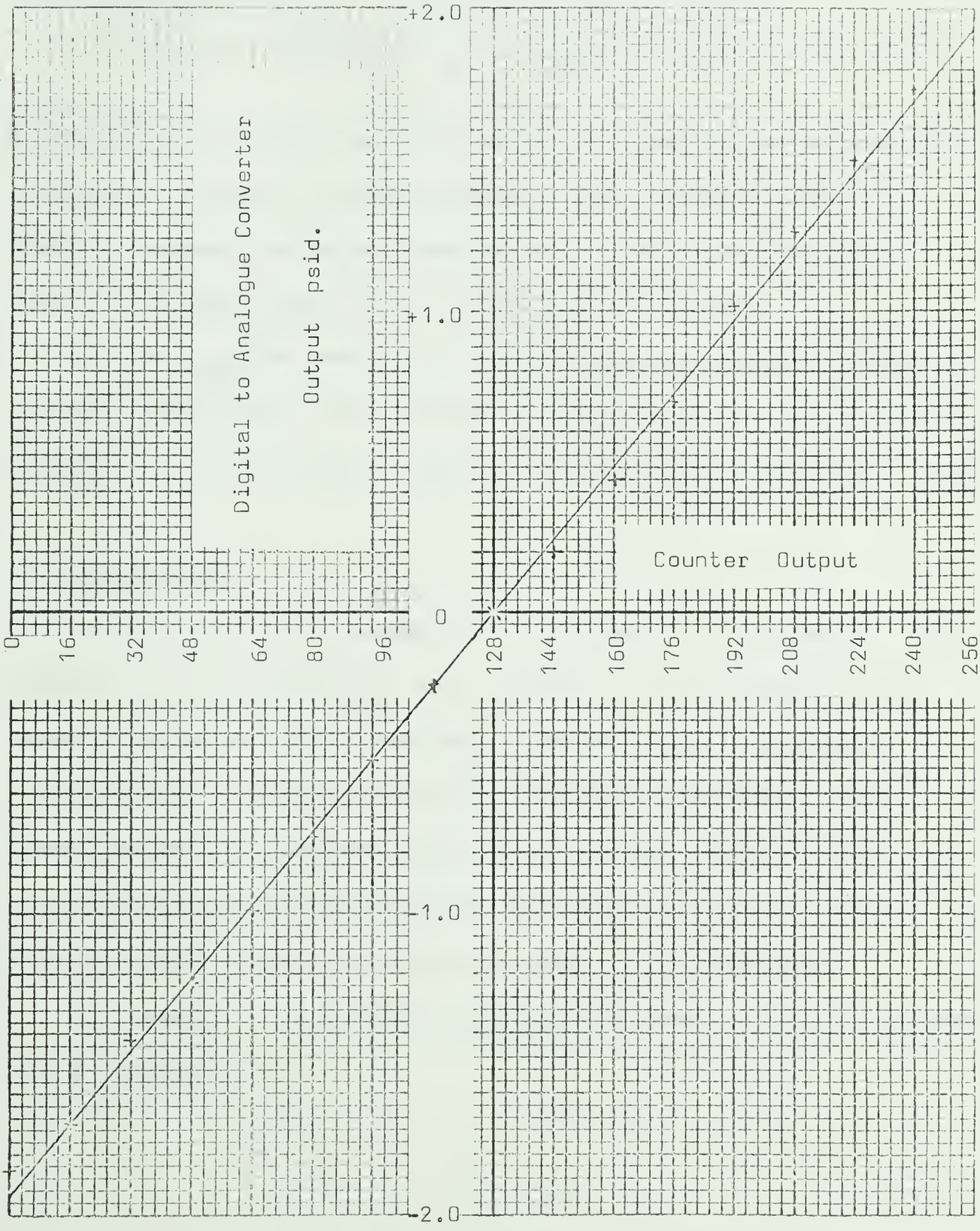
2) The values of the resistances associated with each input form a geometric progression with ratio 2.

Under these circumstances, when P_1 goes on ($0 \rightarrow P_i$) it causes twice the increase in P_s that is caused by P_2 going on. P_s can thus take a series of equally spaced discrete values determined by the state of P_1, P_2, . . . P_n.

For P_s to be able to take values of a sufficiently large size R_t must be large in comparison with the parallel combination of input resistances. This means that loads with low input impedance cannot be driven. An operational amplifier is therefore used as a buffer. The circuit is shown in Fig. 6.2.



Digital to Analog Converter Circuit Fig. 6.2



Digital to Analogue Converter Performance Fig. 6.3

The flip-flops are the logic output stages of the UP-DOWN counter. P_i has a value of 1.5 psig. Other component values were chosen as follows:-

R_f	= 120 RU	R_3	= 16 RU
R_i	= 20 RU	R_4	= 32 RU
R_1	= 4 RU	R_5	= 64 RU
R_2	= 8 RU	R_6	= 128 RU

$$R_t = 2RU$$

R_f was chosen to provide as much feedback as possible, consistent with stability, in order to obtain the most linear response. With their component values, the output range of the converter is $\pm$1.8 psid., which is the most linear part of the amplifier's range.

R_{b1} and R_{b2}, the resistors of the biasing network are chosen so that the differential output pressure is zero when the counter state is 1000000. R_{b2}, the variable resistor is a needle valve having a 1° taper.

6.2 Performance

The accuracy of the conversion is limited by the linearity of the amplifier and the accuracy of the resistors. The tolerance of the resistor values is $\pm$10%, which means that the potential degree of non-linearity from this source alone is 22% of the full scale. Only by careful choice of components can this be avoided. Fig. 6.3 shows the results obtained with the converter which was built. The maximum departure from linearity was 5%, much better than predicted.

The output of the Digital to Analogue Converter provides the output of the integrator.

CHAPTER 7

OVERALL PERFORMANCE

7.1 Integrator Gain

The integrator gain, the rate at which it integrates in a system, is determined by four factors:-

1) The count pulse rate

2) The input range of the Pulse Width Modulator and the output range of the Digital to Analogue Converter

3) The number of counter stages employed

4) The gain of any valves or amplifiers fed by the output of the D to A converter.

The fourth factor is outside the field of interest of this thesis, so that only the gain up to the output of the D to A converter will be considered. If the input pressure range of the PWM is L psi and the count pulse frequency is f_c Hz then when the input to the PWM is 1 psi greater than the mid-range value the UP count rate, R, is given by:-

$$R = f_c \times \frac{1}{L/2} \text{ counts/psi/sec} \qquad (7.1)$$

If the number of counter stages is n its output range is 2^n. If the range of the D to A Converter is M psid. then the gain of the converter, K_c, is given by:-

$$K_c = \frac{M}{2^n} \text{ psid/count} \qquad (7.2)$$

The gain of the integrator, K_i, is then given by:-

$$K_{id} = RK_c = \frac{f_c L}{M \times 2^{n-1}} \text{ /sec} \qquad (7.3)$$

if the output of the D to A Converter is used differentially, and by:-

$$K_{iz} = \frac{RK_c}{z} = \frac{f_c L}{M \times 2^n} \text{ /sec} \qquad (7.4)$$

if a single sided output is used. As built the system described in this thesis had the following parameter values:-

f_c = 8Hz M = 3.6 psid.
L = 3 psi. n = 8

so that:-

K_{id} = 0.0348/sec
K_{iz} = 0.0174/sec

In order to decrease the gain there are two alternatives. The count pulse frequency (and also the frequency of the PWM wave) can be decreased, which is not feasible without considerable increase in the bulk of the circuit. However, the same effect can be achieved by an increase in the number of counter stages. On the other hand, the gain can be increased by an increase of up to one hundred times in the count pulse and sample rates.

7.2 Power Consumption

One disadvantage of the fluidic approach is that there is a steady consumption of compressed air by each of the active devices in the circuit. The rate of air flow to each of the components of the system is:-

Low frequency square-wave generator (1)	—	0.46 SCFM
High frequency square-wave generator (1)	—	0.26 SCFM
Operational amplifier (2)	—	0.20 SCFM
Counter stage (8)	—	0.72 SCFM
Schmitt trigger (3)	—	0.35 SCFM

so that the total air consumption of the integrator is approximately 8 SCFM. This compares with a conventional "force balance" type

pneumatic PID controller having a consumption of 0.5 SCFM.

7.3 Air Supply Regulation

The basic supply pressure for the entire system is 15 psig. Where supply pressures lower than this are needed for specific sections of the circuit, needle valves are used to obtain the reduction. For proper functioning of the circuit the regulation of the basic supply pressure must be less than $\pm$0.5 psi. If it is outside this range the operational amplifiers cease to function satisfactorily.

The air supply must be oil and moisture free; solid particles must be filtered to 20 micron. The ambient air, also, should be clean, to prevent dirt being inducted into the devices from the surrounding atmosphere.

7.4 Conclusion

The fluidic integrator described in this thesis has a potential for application in a number of pneumatic control systems currently relying upon conventional controllers. There is a certain amount of inconvenience in adjusting the integrator rate, but this would be decreased by the use of variable capacitors. These could be cylindrical in shape with pistons to adjust their volumes. It would then only be necessary to change each of the capacitors in the circuit so that the ratios between them remain constant. To obtain lower integration rates additional counter stages could be added to the UP-DOWN counter quite simply, if properly designed.

The integration rate is lower for small signals than for larger ones, due to the sampling and counting technique employed. This effect can be reduced by increasing the count frequency to sample

frequency ratio, but it would then be necessary to use a greater number of counter stages. This is necessary so that for the same sampling frequency the integration rate will remain constant, and the intersample ripple on the output of the Digital to Analogue Converter will not be increased.

The large air consumption of this system, nearly 15 times greater than that of a conventional PID pneumatic controller might be a serious disadvantage in many applications. However, as a component in a process where the air consumption of the rest of the plant is already large, the inherent reliability of the fluidic approach may put it at an advantage.

Although bulky in its individual component form, one of the features of fluidic circuits is that they can be integrated into monolithic blocks having appreciably less bulk than the prototype design.

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APPENDIX A

FLUIDIC ACTIVE DEVICES

A.1 Devices Used

The circuits described in this thesis were all designed around and built with the range of standard fluidic active devices manufactured by Corning Fluidic Products, a department of Corning Glass Works. The devices employed were:-

Part No.	Function
FD 2511-2-1211	Proportional Amplifier without centre dump
190807	Centre Dump Proportional Amplifier
190815	"OR-NOR" gate
FD 2211-2-1211	Bistable device. Load sensitive.
190415	Bistable device. Load insensitive.
190462	Schmidt Trigger.
190999	Single Stage Binary Counter.

A.2 Operating Principles

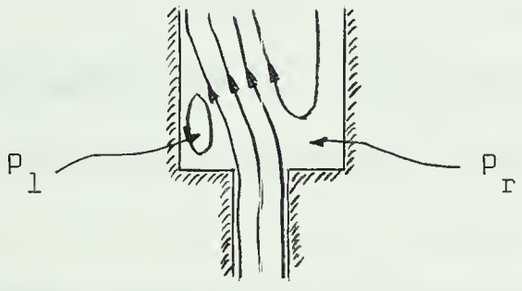
Each of the above devices depends for its operation on one or both of two operating principles. These are the Wall Attachment (Coanda) effect and the Jet Deflection effect. These are not the only fluid-dynamic phenomena which have been applied in the development of fluid amplifiers, but these are the ones which apply for the devices employed in this project. They will therefore be described in further detail.

A.3 The Coanda Effect

The basic Coanda, or Wall-Attachment phenomena may be observed in the pouring of a liquid down a stick held at some angle to the vertical. (Fig. A.1) It will follow the stick rather than flow vertically downwards.

Basic Coanda Effect as Seen in Flow of Liquid over a Stick Fig. A.1

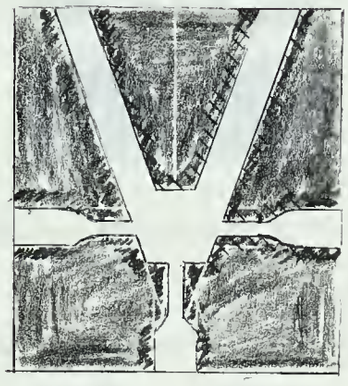
As applied in two state fluid amplifiers (the Bistable elements, and the OR-NOR gates used in this project) it refers to a jet exiting from a two-dimensional nozzle into a wider but still confined two-dimensional flow passage. The jet will attach itself to one wall or the other of the wider passage. (Fig. A.2)



Coanda Effect with Two-Dimensional Jet Fig. A.2

The explanation of the Coanda effect is that fluid is entrained by the jet from the fluid on either side. The entrained fluid must be supplied by a reverse flow along the walls of the chamber. If the jet deviates towards one wall the passage along that wall for the reverse flow is narrowed. As a result, the pressure immediately downstream of the nozzle exit on this side, P_l, is reduced, while P_r rises. This pressure differential acts as positive feedback, increasing the deviation until the jet is completely attached to the wall. The introduction of fluid from some other source into the pocket of trapped fluid on the side of attachment raises the pressure, P_l in this case, enabling the jet to detach, and, if raised sufficiently high, forcing it to attach itself to the opposite wall.

It is this phenomenon which is used in the bistable devices, and the OR-NOR gate. The bistable devices are symmetrical in shape, Fig. A.3, so that each side is equally stable.



Basic Wall-Attachment Bistable Element Fig. A.3

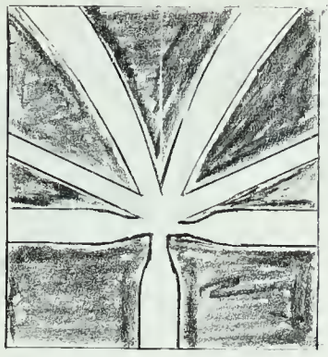
In the monostable OR-NOR gate there is a large vent on one side which prevents attachment to that wall unless driven by input from the opposite side.

In the wall attachment amplifier the flow is directed into one of two output ports, depending upon which wall it is attached to, by the beam splitter. Because the stagnation pressure of the main flow is considerably greater than the control pressure required at the control ports to switch the jet, pressure amplification results. Flow and power amplification are also produced. The characteristics of the amplifier are dependent upon its geometry (Ref. 8, 9 and 10). In general it is found that the gain is inversely proportional to the degree of stability.

A.4 Jet Deflection Effect

The jet deflection amplifier is a proportional device producing a differential output as a result of a differential input. In configuration it is similar to the wall attachment amplifier except that the wall is removed in the region immediately downstream of the power jet nozzle, where

attachment would otherwise occur. (Fig. A.4)

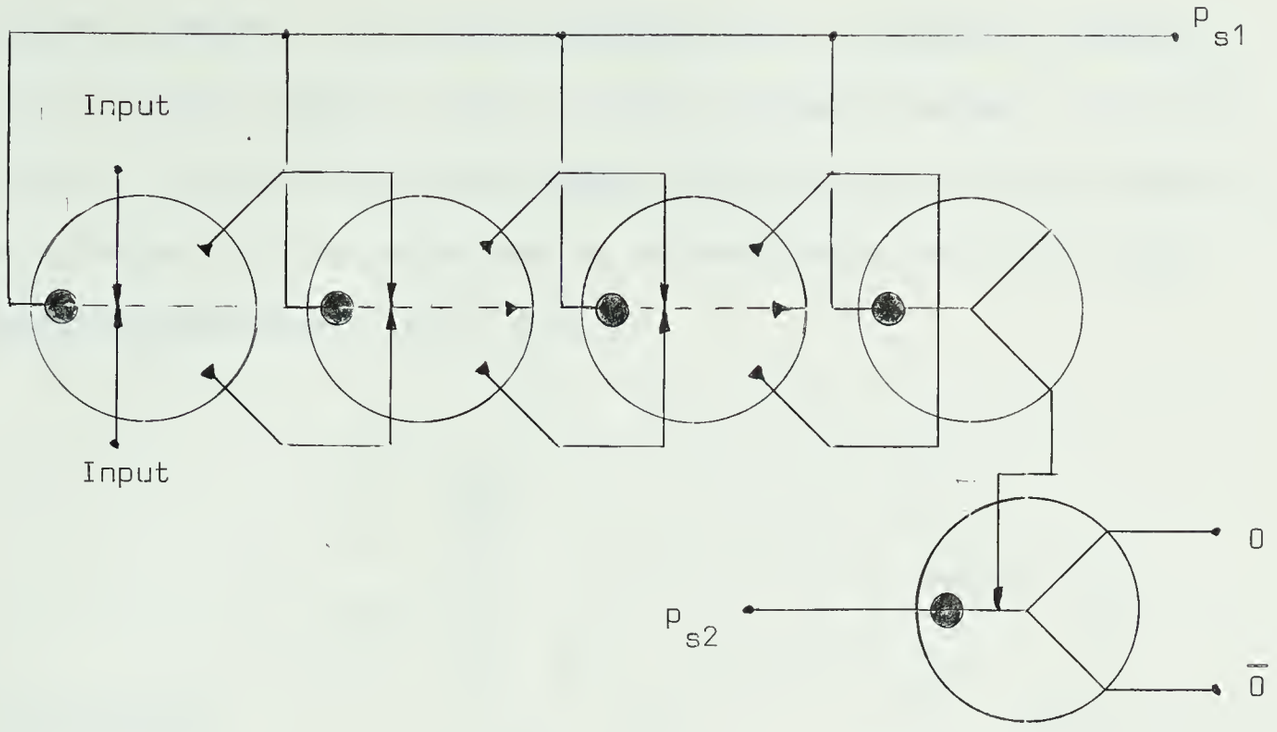


Jet Deflection Amplifier Configuration Fig. A.4

With no input the power jet splits equally between the two outputs to give equal pressure and flow, and therefore zero differential output, assuming a balanced load. The introduction of a pressure at one or other of the control ports causes the jet to deflect toward the opposite output resulting in an increase in the pressure and flow in this port and a decrease on the other side. A differential output is thus produced. Gain results because the change in the output signal is larger than the change in the differential control signal. The actual mechanism of deflection of the jet may be differential pressure gradient, or momentum transfer, or a combination of the two, depending upon the geometry of the element. (Ref. 11, 12).

A.5 Schmitt Trigger

The Schmitt trigger utilizes three proportional amplifiers in cascade to provide high gain,with the final stage switching a bistable element. The purpose of the proportional stages is to overcome the hysteresis of the bistable element, so that the final trigger has virtually no hysteresis. The bistable element switches an OR gate which provides a final stage of gain and a load insensitive output. Fig. A.5 is the schematic circuit of the Schmitt trigger.



Schematic of Schmitt Trigger Circuit Fig. A.5

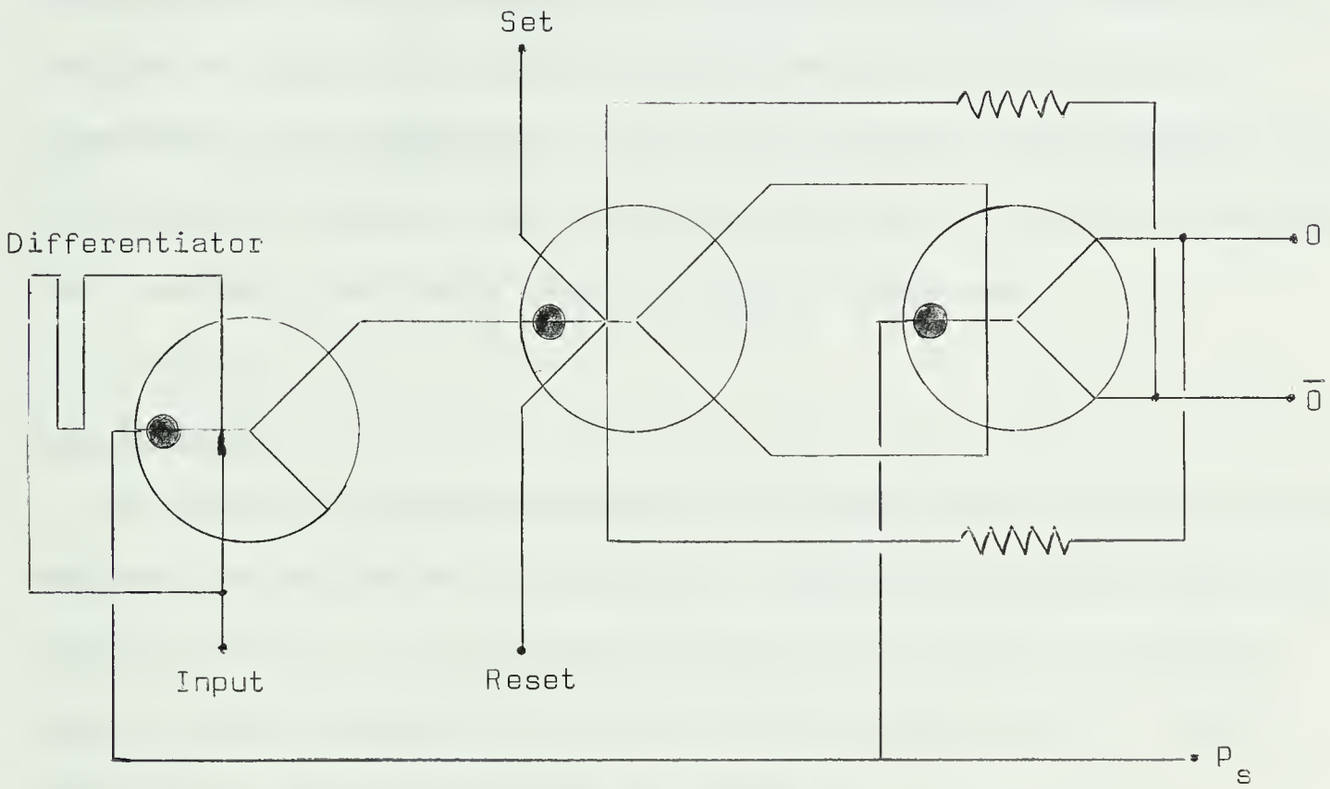
This circuit has been integrated into one device by Corning. The performance data for the device is as follows:-

	Norm	Max	Min
Supply Pressure I	1 psig.	2 psig.	0.5 psig.
Supply Pressure II	3 psig.	6 psig.	1.5 psig.
Switch Pressure	1% to 35% of Supply Pressure I		
Supply Pressure Ratio I:II	1:3 for Low Frequency 1:1 for High Frequency		

A.6 Binary Counter

The binary counter used in this project contains three active elements. The input is fed to both sides of a monostable element. One input feeds directly, causing the element to switch to the unstable side, while the other input is delayed 0.0006 secs. before it causes the element to switch back to its stable position. As a result, provided that the input has a sufficiently sharp rise, a pulse of 0.0006 second will appear on the unstable output. This pulse is fed as the supply to a

bistable element. The output of this element is biased by feedback from the final element, which is another bistable device. The output from the first bistable is the input to the second, and the feedback is so arranged that the second device is always switched by the output pulse from the first. (Fig. A.6)



Circuit of Binary Counter Device. Fig. A.6

Two further inputs to the first bistable element are SET -RESET inputs.

APPENDIX B

FLUIDIC PASSIVE COMPONENTS

B.1 Application

In fluidic analogue circuits, as in electronic circuits, passive components are used to produce the required performance. Ideally as in the case of electrical circuits, the performance of the circuit is independent of the parameters of the active devices. This situation is not achieved in practice due to the shortcomings of the active components, their low gain, and finite input and output impedances.

B.2 Resistors

The fluidic resistive equivalent is a restriction in the flow passage. Resistors may be linear or non-linear. Linear resistors are formed from capillary tubes of the requisite bore, length and number. Non-linear resistors may be formed by any type of restriction, such as a needle valve. The definition of fluidic resistance is:-

$$R = \frac{Pd}{Q} \qquad (B.1)$$

where:-

Pd = Pressure drop in psid.
Q = Mean flow rate measured in standard cubic inches/sec.

The unit of resistance is lb sec/in^5, termed the Resistance Unit (RU) in this thesis.

B.3 Capacitors

No fluidic equivalent exists for the electrical point to point

capacitor which does not require moving or deformable parts. However, any volume is the equivalent of a shunt capacitor to ground. The formula for capacitance is:-

$$C = \frac{dM}{dP} \qquad (B.2)$$

where:-

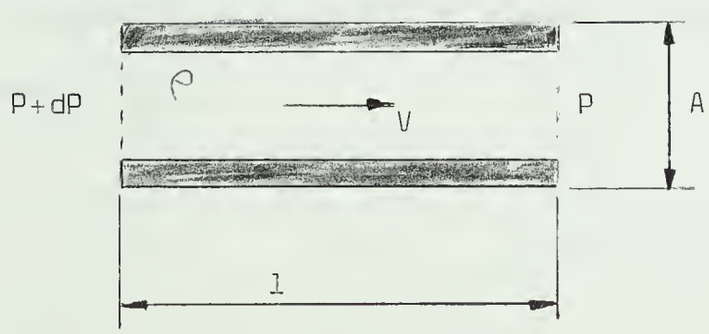
dM = Change of mass of air contained in the volume, in standard cubic inches

dP = Change of pressure inside the volume, in psi.

The unit of capacitance is in^5/lb, called the Capacitance Unit (CU) in this thesis.

B.4 Inductors

Inductances are normally avoided if possible in electronic circuits, and the same is true of fluidic circuits. There does, nevertheless, exist an equivalent of self-inductance, but none of mutual inductance. The inductance results from the inertia of a mass of gas enclosed in a long tube and a formula may be derived for its magnitude.



Fluidic Inductance Fig. B.1

l = length of tube
ρ = density of fluid
A = area of flow passage
V = velocity of flow

It is assumed that P is sufficiently small that ρ is constant throughout the length of the tube so that:-

$$Q = A\dot{V} \qquad (B.3)$$

$$AdP = \dot{V}lA \qquad (B.4)$$

Inserting equation (B.3) in (B.4):-

$$dP = \frac{\rho l}{A}d\dot{Q} \qquad (B.5)$$

so that the fluidic inductance L is given by:-

$$L = \frac{dP}{\dot{Q}} = \frac{\rho l}{A} \qquad (B.6)$$

The unit of inductance is lb/in^5. It is clear, however, that a length of tubing cannot form a pure inductance. The narrower the flow passage the larger will be the resistive component; the larger the flow passage the larger the capacitive component.

B.5 Transmission Lines

Because a long length of pneumatic tubing has both capacitance and inductance it forms a fluidic transmission line. The propagation velocity is the velocity of sound in the constricted fluid, and ideally the characteristic impedance of the line is resistive as for an electrical transmission line.

APPENDIX C

UNITS

The science of fluidics is characterized by a lack of standardization. This extends to the system of units to be employed in the description of devices and circuits. Different workers in the field vary in their choice of basic dimensions and units. For this thesis the basic dimensions were chosen as force, length and time. The units in which each of these were measured were as follows:-

Force - pounds force
Length - inches
Time - seconds.

The circuit quantities and their units are listed in Table C.1.

QUANTITY	ELECTRICAL EQUIVALENT	UNIT	ABBREVIATION
Pressure	Potential	Pounds/square Inch Guage	psig
Differential Pressure	Potential Difference	Pounds/square Inch Differential	psid
Flow	Current	Standard Cubic inches/second	scis
Mass	Charge	Standard Cubic Inches	sci
Resistance	Resistance	1 lb. sec/in^5 = 1 Resistance Unit	RU
Capacitance	Capacitance	in^5/lb = Capacitance Unit	CU
Inductance	Inductance	lb/in^5 = Inductance Unit	IU
Power	Power	Pound Inches	

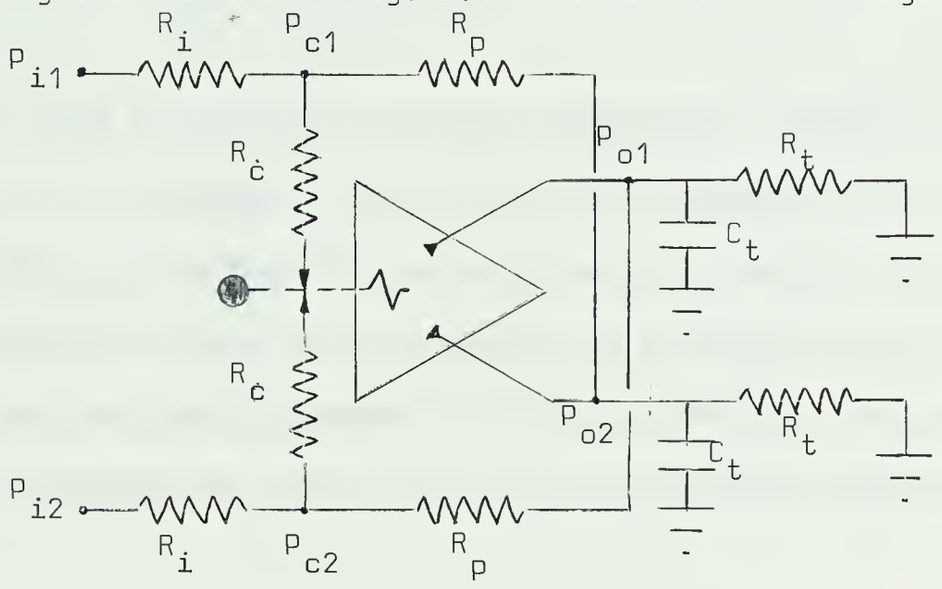
As can be seen the units of flow and mass are to a large extent a compromise between measuring the flow in mass units or in volumetric

units. Each has its advantages. If the volumetric measure were used then the product Pressure x Flow would have the dimensions of Work. However, in a compressible fluid volume is not an absolute quantity. There is, on the other hand, a law of conservation of mass, which makes possible the writing of node equations for flow. The compromise is to use the Standard Cubic Inch, being the mass of gas having a volume of one cubic inch at standard temperature and pressure. Provided that the temperature and pressure do not deviate too greatly from the standard, the mass measurement in standard cubic inches is close to the volumetric measurement.

APPENDIX D

BOOTSTRAP INTEGRATOR

Bootstrap integrator circuits have been described in Refs. 13 and 14. The circuits depend upon the use of positive feedback, and an attempt was made using the circuit of Fig. D.1 to build such an integrator.



Experimental Bootstrap Integrator Circuit Fig. D.1

The condition that this circuit will integrate is that under zero differential input pressure the steady state differential output pressure be indeterminate. The circuit equations are:-

$$\frac{P_{cl} - P_{il}}{R_f} + \frac{P_{cl}}{R_i} + \frac{P_{cl} - P_{or}}{R_f} = 0 \qquad (D.1)$$

$$\frac{P_{cr} - P_{ir}}{R_i} + \frac{P_{cr}}{R_c} + \frac{P_{cr} - P_{ol}}{R_p} = 0 \qquad (D.2)$$

These may be combined:-

$$\frac{-P_{id}}{R_i} + \frac{P_{cd}}{R_c} + \frac{P_{cd}}{R_p} + \frac{P_{od}}{R_p} = 0 \qquad (D.3)$$

If the gain of the amplifier is G, then:-

$$P_{od} = -GP_{cd} \qquad (D.4)$$

so that:-

$$\frac{-P_{id}}{R_i} + P_{cd}\left(\frac{1}{R_c} + \frac{1}{R_p}(1 - G)\right) = 0 \qquad (D.5)$$

which indicates that for $P_{id} = 0$, the condition for P_{cd} (and P_{od}) to be indeterminate is:-

$$\frac{1}{R_c} + \frac{1}{R_p}(1 - G) = 0 \qquad (D.6)$$

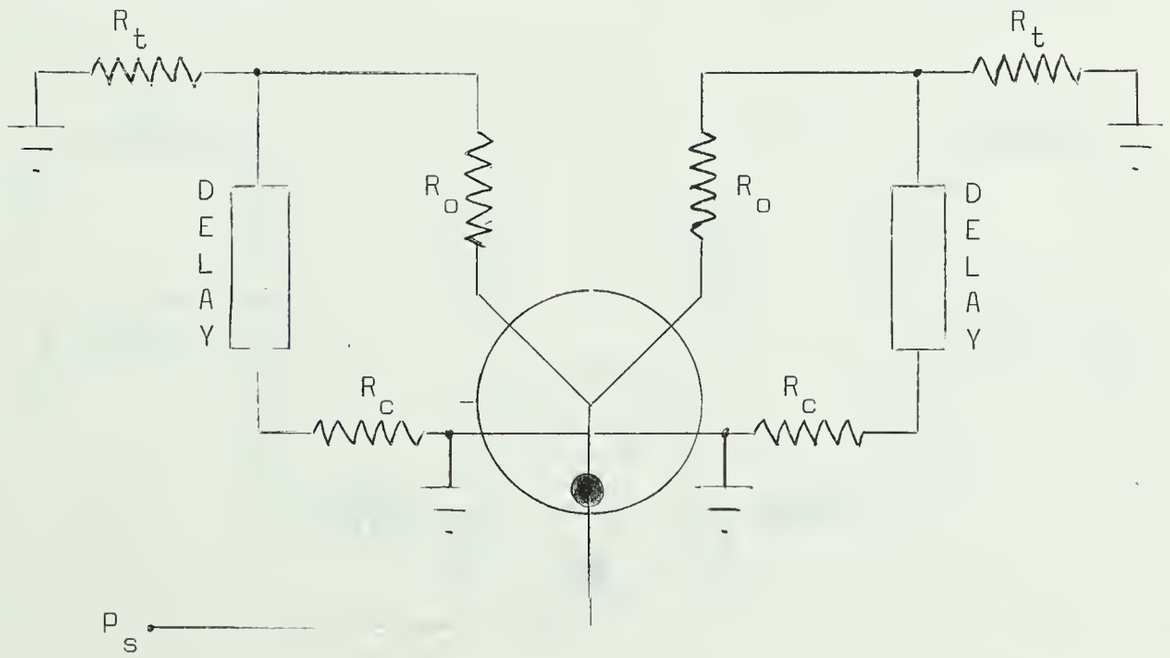
It was found experimentally nearly impossible to satisfy this condition. It is necessary that G be constant throughout the output range, and that both R_p resistors be adjusted to exactly the right value. The first condition could not be satisfied by the amplifier as designed, and the second required adjustment of infinite precision, so that this circuit was dismissed as impractical with the available components.

APPENDIX E

HIGH FREQUENCY PULSE GENERATOR

The frequency of oscillation of the square wave generator described in Chapter 2 is increased by reduction of the values of C_c and R_f. However, as the frequency increases a point is reached at which the lumped perameter analysis of Section 2.2 no longer applies. Delays are introduced by the interconnecting tubing, and these must be considered. In the high frequency multivibrator described in this appendix the switching time is determined by the length of the delays.

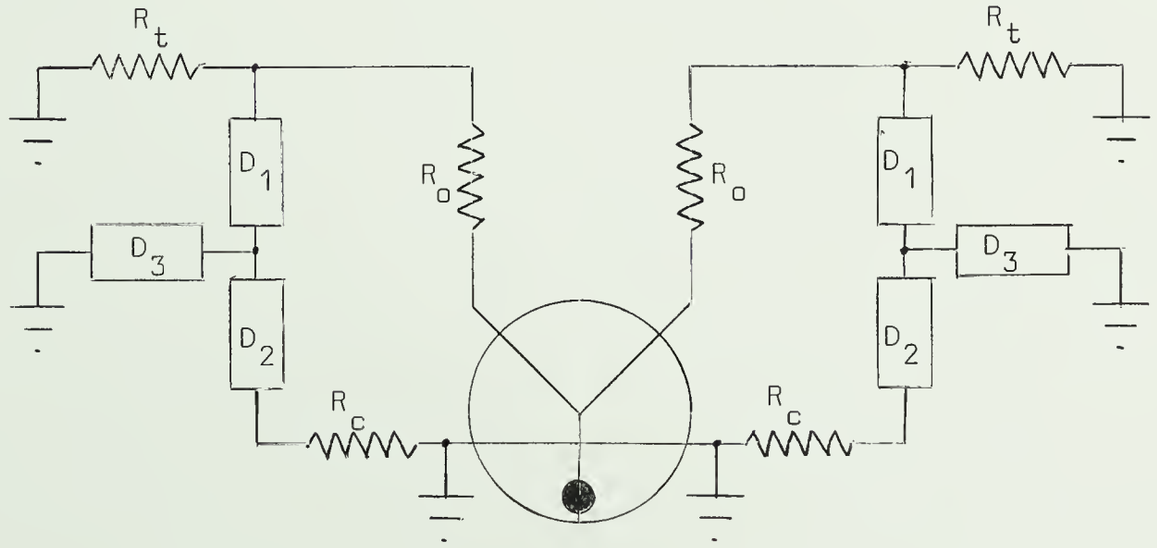
The propogation velocity of disturbances through the tubing interconnecting fluidic devices may be assumed to be approximately 1000 ft/sec, so that the delay introduced is 0.0833 m sec/in. The simplest multivibrator working on the sonic delay line principle uses lines feeding directly back to the input from the output, as in Fig. E.1.



Equivalent Circuit. Simple Delay-Line Multivibrator. Fig. E.1

The delay lines are 0.125 in. I.D. tubing, which if assumed lossless, has a characteristic impedance of 1.17 RU. The switching time of the bistable element is 0.5 m sec. With this arrangement the minimum length of interconnecting tubing which could be used was 6 ins. A frequency of 260 Hz was produced. It was impossible to make reliable measurements since the measuring equipment introduces additional capacitance which significantly alters the circuit. Without such measurement any analysis of the mechanism of operation based on the actual performance of the system and the physical dimensions can only be speculative, but may be instructive. Operating at 250 Hz the delay between the ON and the OFF pulses on one side of the flip-flop is 2 m sec. 0.5 m sec. is accounted for by the switching time of the device, so that 1.5 m sec. must be due to the delay line. 1.5 m sec. is the time required for a pulse to travel up and down the line three times, which indicates that two reflections must occur before sufficient differential pressure is produced at the control inputs to cause switching.

A modification to the basic scheme above is illustrated by Fig. E.2.



Equivalent Circuit. More Complicated Delay-Line Multivibrator. Fig. E.2.

This arrangement is even more difficult to analyze without measurements. A maximum frequency of 480 Hz was obtained when each delay was made 3 ins. long. This means that the delay caused by the lines is now only 0.5 m sec., indicating that the switching pulse travels down the two delays (1) and (2) only once. A complicated interaction must occur between the pulses in the three lines.

The theoretical maximum frequency of oscillation is determined by the switching time of the device itself, so that 1000 Hz is the upper limit. However, 6 ins. of interconnecting feedback tubing is the minimum made necessary by the geometry of the device. A practical upper limit is therefore 500 Hz. Even this may be a higher frequency than can be advantageously used. Although the theoretical frequency response of devices driven by the multivibrator is also 1000 Hz this can be achieved only with the most careful loading. The maximum frequency which could be used without encountering this problem was 70 Hz.